

Demonstration of Silicon Carbide Power Devices in Practical Power Conversion Systems

Grant No. N00014-01-1-0077

Final Technical Report

Submitted to the

Office of Naval Research
Electronics Division, Code 312
800 North Quincy Street
Arlington, VA 22217-5660
Attn: Dr. Ingham Mack

Submitted by

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January 12, 2005

1. Introduction

The goals of this project are: (1) to develop a design and processing sequence for high-power 4H-SiC bipolar junction transistors (BJTs) with blocking voltages above 1,000 V and on-state currents above 25 A; (2) to fabricate and package sufficient quantities of these devices to implement a demonstration motor control system; (3) to design and develop a prototype 40 – 100 kW motor control system for demonstrating the SiC BJTs; and (4) to operate the SiC BJTs in the prototype system as a real-world test of the feasibility of this technology for practical power conversion systems.

This report is divided into five sections. **Section 2** describes the design, fabrication, and characterization of a test wafer, designated *BJT Wafer #0*, that was used to verify the designs and fabrication processes. As will be seen, Wafer #0 taught us a great deal about the optimum design of SiC BJTs, particularly the deleterious effects of the p+ implant used for ohmic contact to the base regions. If this implant is positioned too close to the edge of the n+ emitter, the common emitter current gain is significantly degraded due to recombination of injected electrons at damage sites in the implant. This effect was alleviated in subsequent “production” wafers by positioning the p+ implant at least one diffusion length from the emitter edge. **Section 3** summarizes the results of “production” runs for *Wafers #1 – 6*, fabricated using the optimized “2 kV” BJT design. As will be reported, the BJT devices met operational specifications, but problems were encountered with the top-level metallization during die attach and wire bonding. Since packaging was not explicitly included in the funding for this project, this presented major problems that prevented us from operating large numbers of these devices in the prototype control system. **Section 4** describes the design and operation of the prototype motor control circuit, which was developed and optimized using silicon BJTs as switches in preparation for insertion of the packaged SiC BJTs. **Section 5** summarizes the accomplishments of this project, the current status, and plans for completing the SiC breadboard demonstrations.

2. Fabrication and Experimental Results on the Initial Process-Development Wafer (*Wafer #0*)

This section discusses the design, fabrication, and experimental results of the initial process-development wafer (*Wafer #0*) of 4H-SiC BJTs. To investigate the ability of 4H-SiC BJTs to work as power switches, devices designed to block both 2 kV and 5 kV are fabricated.

2.1 Fabrication of 4H-SiC BJTs

2 inch 4H-SiC wafers with n+/p/n- epilayers on n+ substrates are obtained from Cree, Inc. The layer-by layer doping concentrations for 5 kV devices are $1 \times 10^{19} \text{ cm}^{-3}$ / $2 \times 10^{17} \text{ cm}^{-3}$ / $8 \times 10^{14} \text{ cm}^{-3}$. The layer thicknesses are 1 μm/1 μm/50 μm. The doping concentrations for 2 kV devices are $1.1\text{--}1.5 \times 10^{19} \text{ cm}^{-3}$ / $1.2 \times 10^{17} \text{ cm}^{-3}$ / $2.5 \times 10^{15} \text{ cm}^{-3}$. The thicknesses are 1 μm/1 μm/20 μm.

The samples were first etched 1.1 to 1.2 μm by reactive-ion etching (RIE) in SF₆ to form the base mesas using Ti/Ni/PR as the masking material. The PR is patterned using a different mask. The purpose of the PR is to cover most of the exposed Ni surface to prevent the possible micromasking during RIE process. Another RIE process with the same masking materials was then performed to etch another 1.1 to 1.2 μm to form the emitter fingers. P+ regions under the base contact and the JTE were formed by Al implant at 650°C with zero degree tilt angle. P+ implant doses/energies are $6 \times 10^{13}/40$ and $1.6 \times 10^{14}/130$ (cm⁻²/keV). JTE implant doses/energies are $1 \times 10^{12}/40$, $2 \times 10^{12}/100$, $3 \times 10^{12}/200$, and $5 \times 10^{12}/350$ (cm⁻²/keV) for both 2 kV and 5 kV samples. The implant profiles simulated by TRIM are shown in Fig. 1.

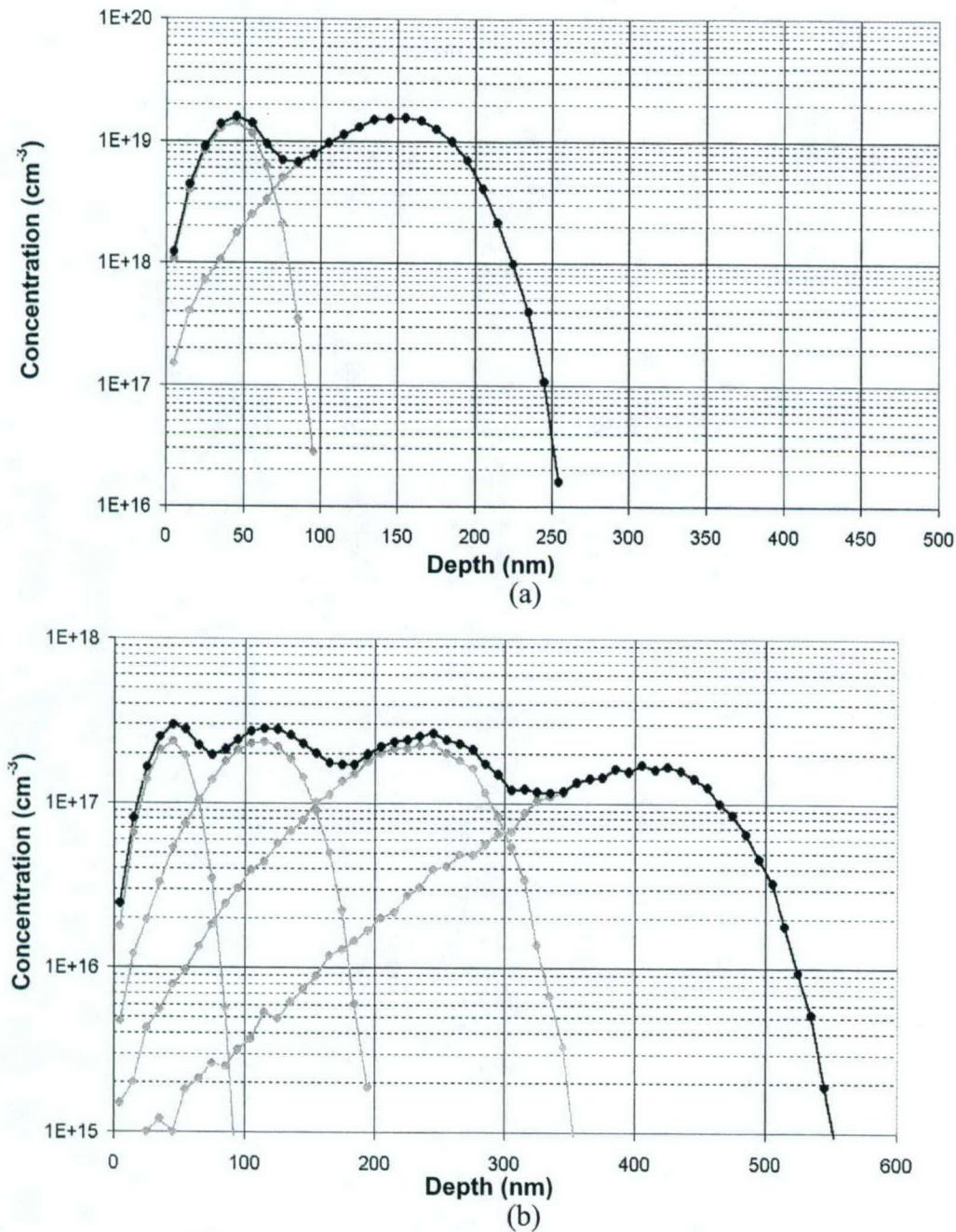


Fig. 1 (a) P+ implant profile; (b) JTE implant profile.

Implant doses were activated by annealing in Ar for 30 min at 1600 °C in an Epigress VP-508 hot wall CVD system without capping. The activation percentage after annealing at this temperature is estimated to be 70-80%. After RCA clean, an MOS gate quality oxide was grown on the samples in a pyrogenic system by wet oxidation at 1150°C for 2.5 hours, followed by

950°C annealing in argon for 1 hour and 950°C wet reoxidation for 2 hour. The oxide thickness is estimated to be 550 Å. This oxidation process is expected to reduce the surface recombination because it is proven to reduce D_{it} at the oxide/SiC interface. However, its effect on the device needs to be further studied. Contact windows were opened by dipping the samples in BHF for 1 minute with photoresist as an etching mask. 1000 Å of Al on 200 Å of Ti (Ti weight percentage around 25) was e-beam evaporated as the p-type contact, and 1000 Å of Ni was evaporated as the n-type contact on emitter fingers and the backside of the samples. Both contacts were annealed at 1000°C for 2 min in 400 torr argon to form p-type and n-type contacts, separately. Top metal, 8000 Å of gold, is deposited to connect the fingers to the probing pads. 5000 Å of gold is deposited on the backside. A process flow is shown in Fig 2. Photomicrographs of two devices with different active areas are shown in Fig 3.

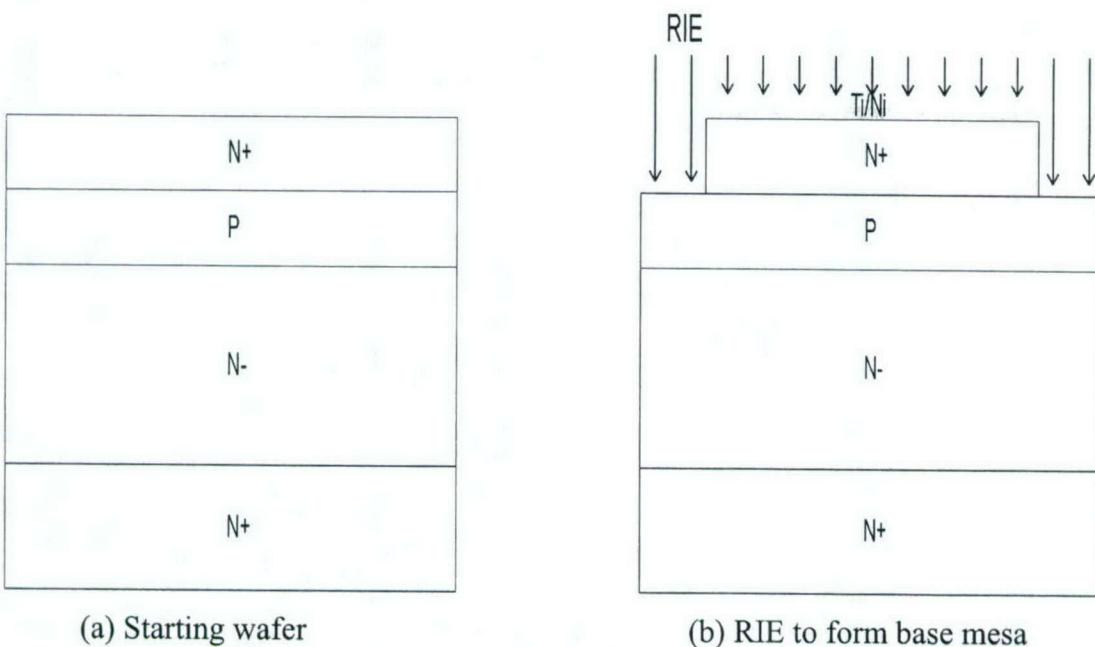
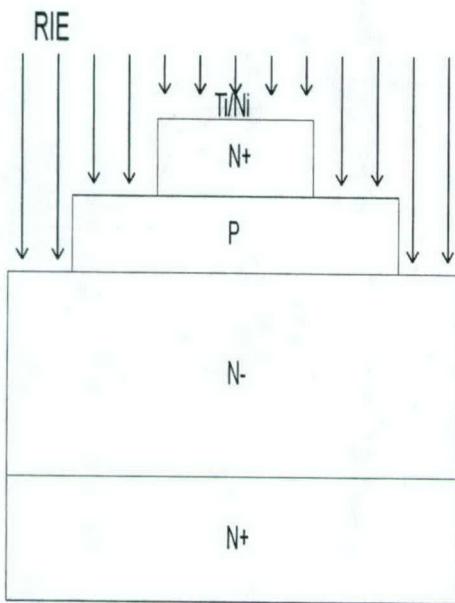
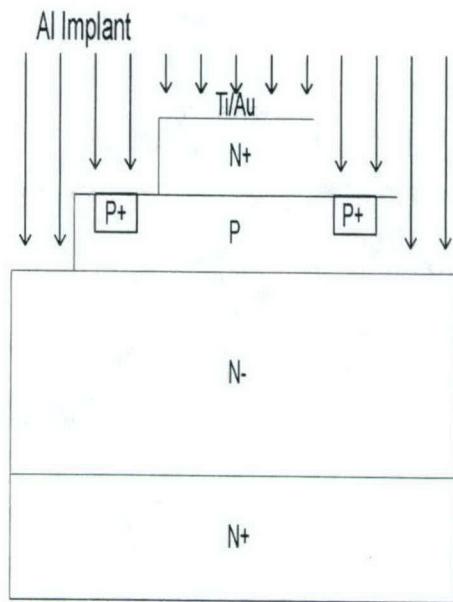


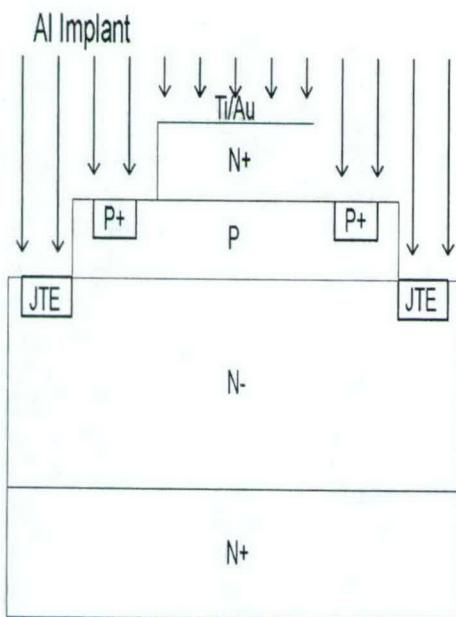
Fig. 2 Fabrication sequence for the SiC BJT process.



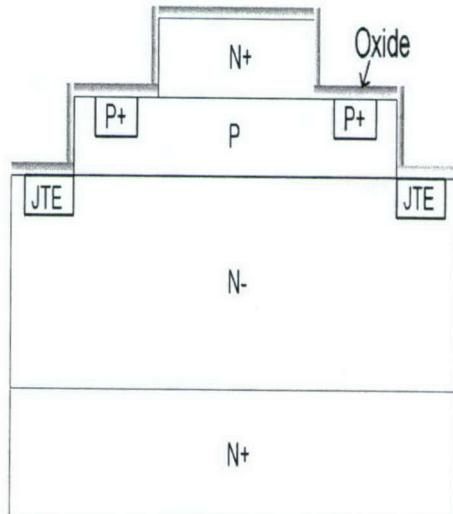
(c) RIE to form emitter fingers



(d) Al implant for p+ region

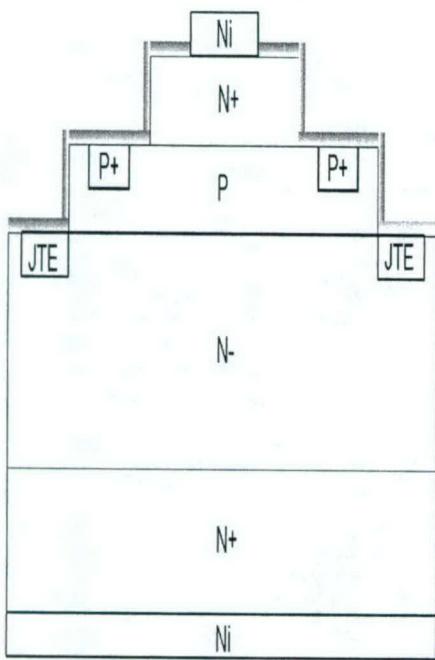


(e) Al implant for JTE

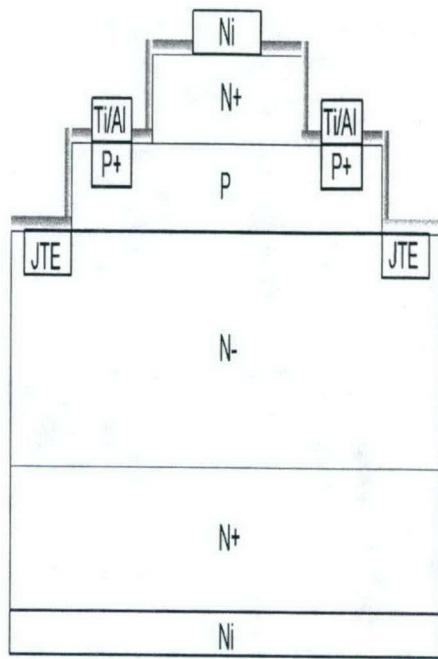


(f) Thermal oxidation for passivation

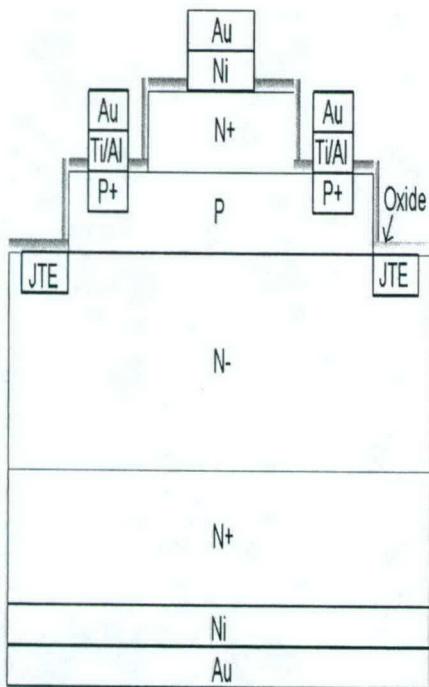
Fig. 2 Continued.



(g) Deposit Ni for n-type contact



(h) Deposit Ti/Al for p-type contact



(i) Deposit Au for top metal

Fig. 2 Continued.

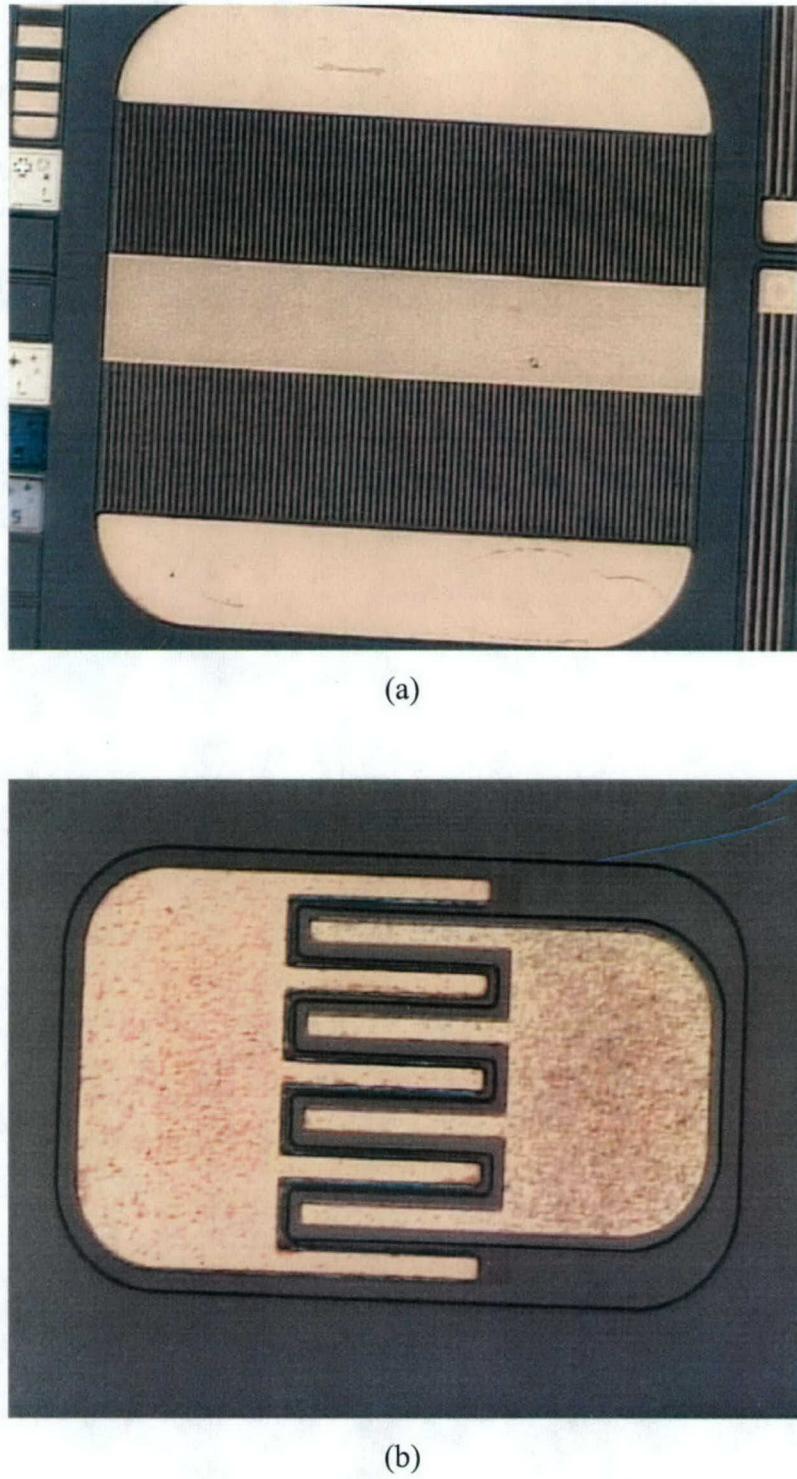


Fig. 3 Photomicrographs of devices after fabrication. (a) a large device with an active area of 1.05 mm^2 . (b) a small device with an active area of 0.0072 mm^2 .

2.2 Device Performance

I-V curves for the devices are extracted using an HP-4156 semiconductor parameter analyzer for small BJTs and TLMs, and a Tektronix 371A power curve tracer and Tektronix 576 curve tracer for large BJTs. Samples are immersed in FlourinertTM, which has a dielectric strength of 40 kV/0.1 inch, to measure high voltage performance. Blocking voltages are extracted using the Tektronix 371A and a custom-made high voltage measurement system. Elevated temperature measurements are performed on a hot chuck which can be heated to 350°C.

2.2.1 TLM measurements

From TLM measurements, the resistivity of contacts can be extracted. As shown in Fig. 4, after 1000°C annealing, both contacts to n+ and p layers are ohmic. From the dimensions of the contact pads (width = 110 μm, length = 50 μm) and the spacing D, n-type contact resistivity ρ_{cn} is estimated to be $4.4 \times 10^{-5} \Omega\text{-cm}^2$, comparable with values reported by others at this doping concentration. Sheet resistivity $R_s = 51 \Omega/\text{square}$ is consistent with the doping and thickness of the n+ layer (1 μm, $1 \times 10^{19} \text{ cm}^{-3}$). Contrary to the uniform distribution of good ρ_{cn} across the wafer, p-type contact resistivity ρ_{cp} fluctuates from spot to spot. The variations in ρ_{cp} may have an impact on specific on-resistance of large BJTs. This will be discussed in more detail later. The best ρ_{cp} measured is $6 \times 10^{-4} \Omega\text{-cm}^2$, as shown in the figure. Average ρ_{cp} is around $3.8 \times 10^{-3} \Omega\text{-cm}^2$. The order of sheet resistivity ($R_s = 1.83 \times 10^4 \Omega/\text{square}$) obtained is also consistent with the doping and thickness in the p layer (1 μm, doped $2 \times 10^{17} \text{ cm}^{-3}$), with partial ionization effects included (8% ionization at room temperature is assumed). The p-type contact resistivity is higher than expected because the p+ implant under the contact should further reduce the resistivity. However, the voltage drop across the p-type contact is estimated to be around 0.1 V if base current density is 25 A/cm², which is low enough for BJT applications.

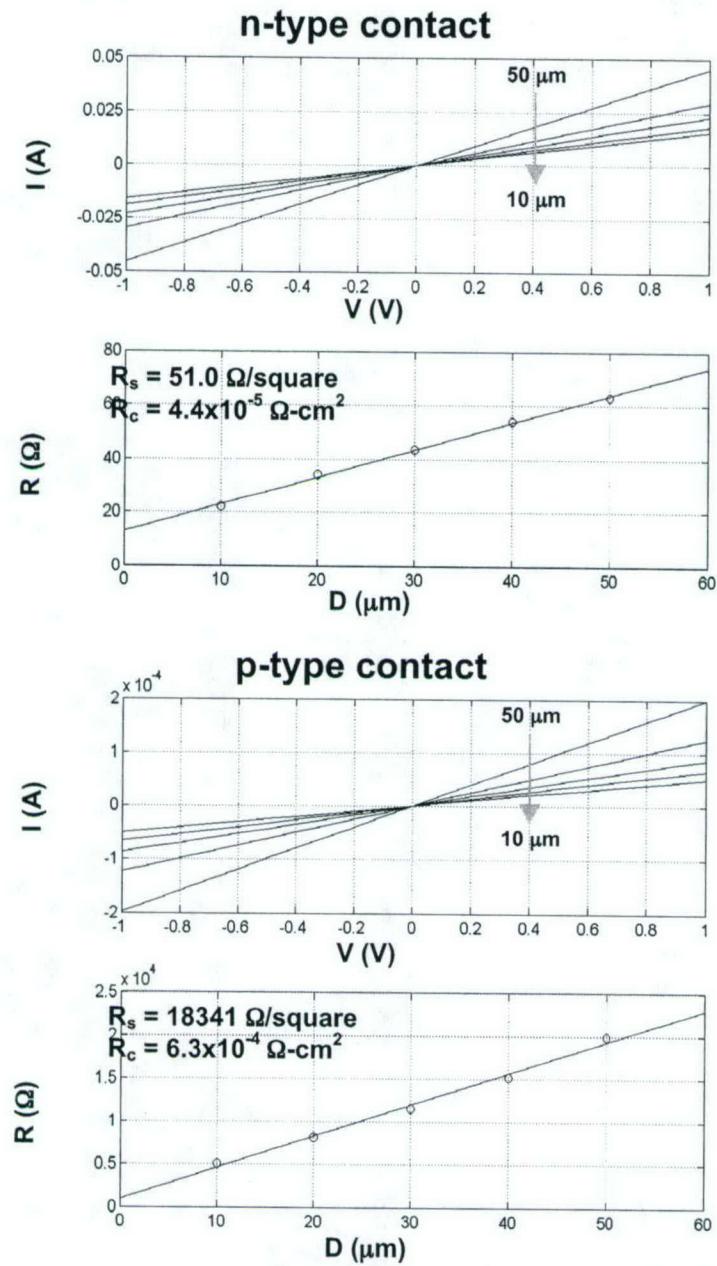


Fig. 4 Contact resistivities from TLM measurements.

2.2.2 2 kV Device performance at room temperature

Figure 5 shows the on-state I-V curves of a device with active area = 1.05 mm², and finger length = 350 μm at room temperature. This device carries 2 A (190 A/cm²) at a forward voltage of 5 V and base current of 50 mA. The current is limited by the fact that current is going

through the probe tip into the device. When the current is large, the local current density will be very large and the probe pad will burn. DC current gain around 55 is observed in the forward active region, which is the highest value reported to date. The specific on-resistance is $26 \text{ m}\Omega \cdot \text{cm}^2$, about 5-6 times the theoretical unipolar value for the collector epilayer. The possible reasons for this high R_{ON} are finger length effect and the non-uniform base contact resistivity effect, which will be discussed in section 2.2.4. Figure 6 shows that BV_{CEO} is 500 V. Figure 7 shows BV_{CBO} around 700 V, 20% of the theoretical value. Before contact anneals, blocking voltage of 1,900 V is obtained from a pn diode structure. This low percentage indicates that blocking voltage is limited by mechanisms other than avalanche breakdown. It is attributed to the punch-through in the base layer caused by aluminum spiking during the ohmic contact anneal and the low base dose. The base dose is $1.2 \times 10^{13} \text{ cm}^{-2}$, which is barely enough to prevent punch-through according to two-dimensional MEDICI simulations. During processing steps such as RIE and oxidation, the base layer under the base contact could be thinned, and the later spiking during contact anneal makes the situation even worse. It is expected that blocking voltage can be further improved by optimizing the base dose and the fabrication process.

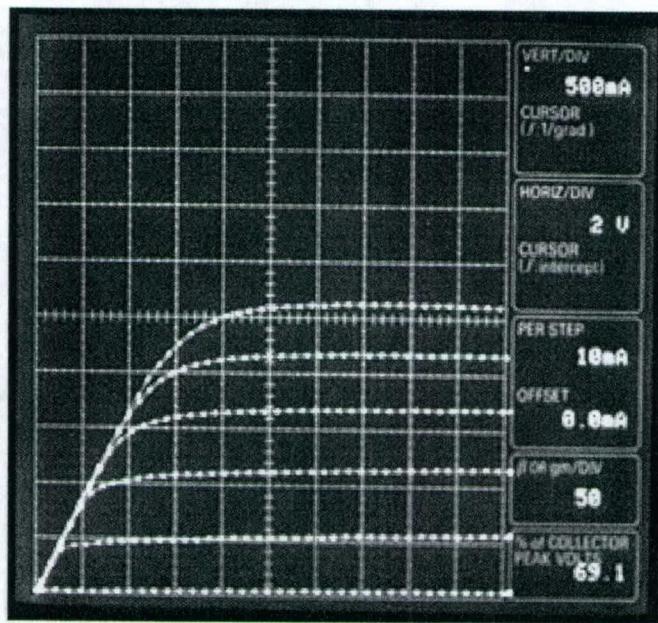


Fig. 5 On-state I-V curve of a large 2 kV device with active area 1.05 mm^2 (finger length = $350 \mu\text{m}$).

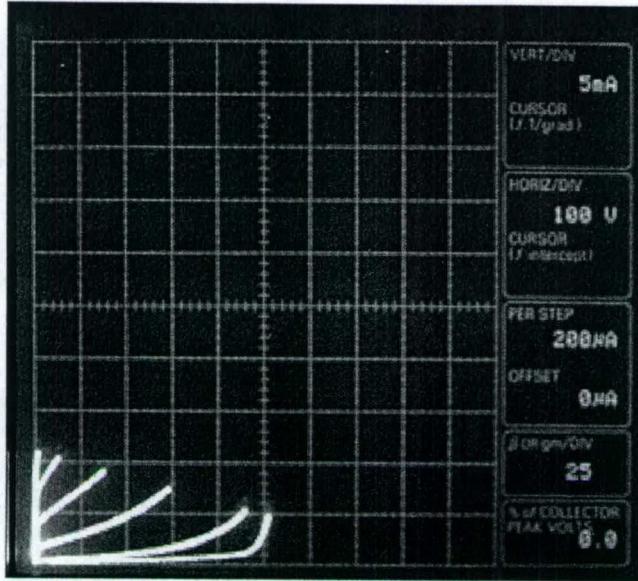


Fig. 6 The device in Fig. 5 shows BV_{CEO} around 500 V.

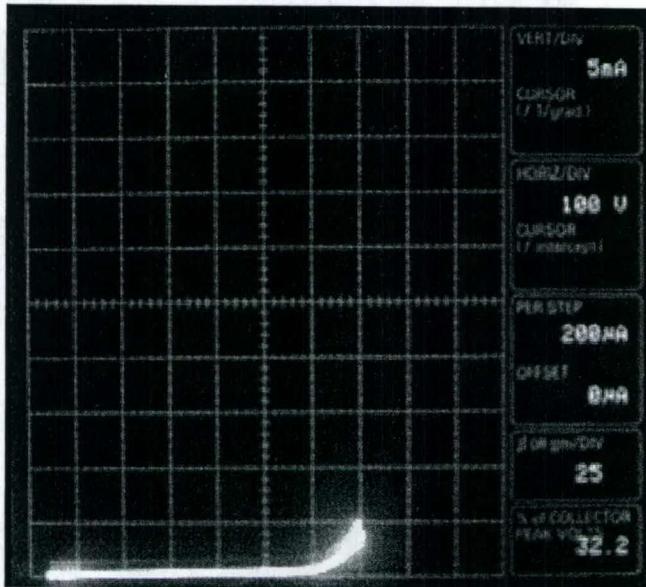


Fig. 7 The device in Fig 5 shows BV_{CBO} of 700 V.

Figures 8-10 show the on-state characteristics of a device with active area of 0.032 mm^2 and finger length of $300 \mu\text{m}$. $R_{on,sp}$ of this device is $8 \text{ m}\Omega \cdot \text{cm}^2$, much smaller than that of the large device. This can be explained by lateral spreading of current in the thick drift region in the small size device, and possibly some conductivity modulation of the drift region. The ideality

factor for base current η_B is close to 2, indicating the base current is dominated by recombination. The collector current, on the other hand, is dominated by $\eta_C = 1$ diffusion current. This device maintains beta greater than 40 up to collector current densities of 700 A/cm^2 , as can be seen in Fig 10. This current density is limited by $R_{ON}V_{CE}$ of the device, above which the device enters saturation and the current gain is dramatically reduced because the base-collector junction is forward biased and base current flows into collector as well as into the emitter.

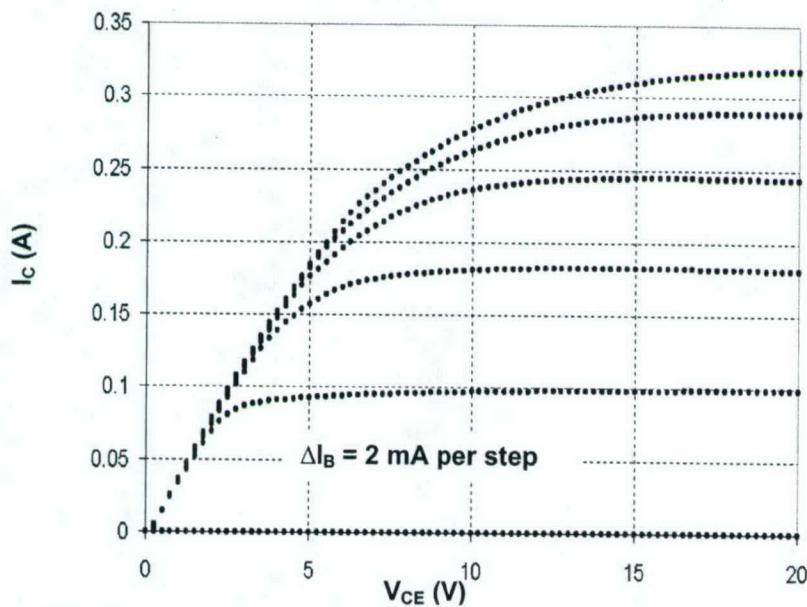


Fig. 8 I-V curve of a 2 kV device with active area 0.032 mm^2 (finger length = $300 \mu\text{m}$).

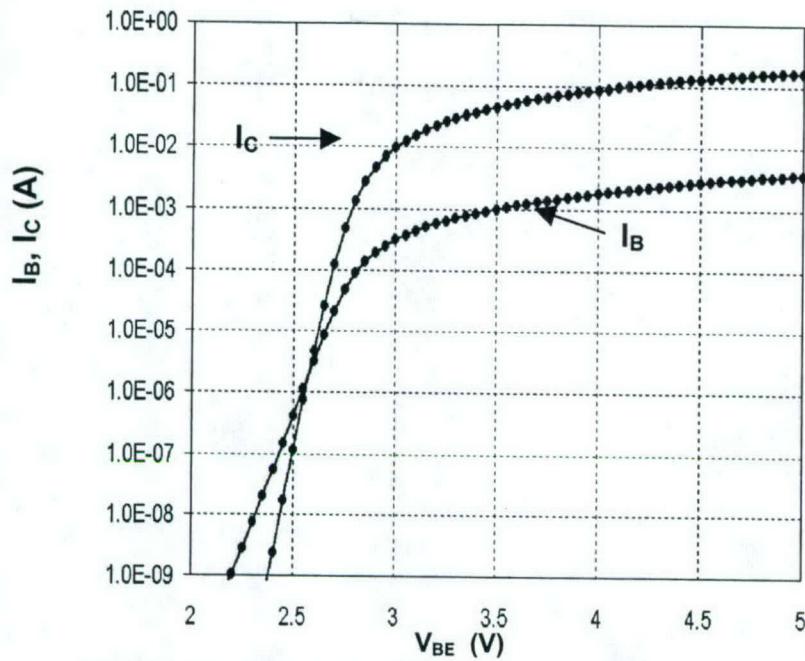


Fig. 9 Gummel plot of the device in Fig. 8 ($V_{CE} = 10$ V).

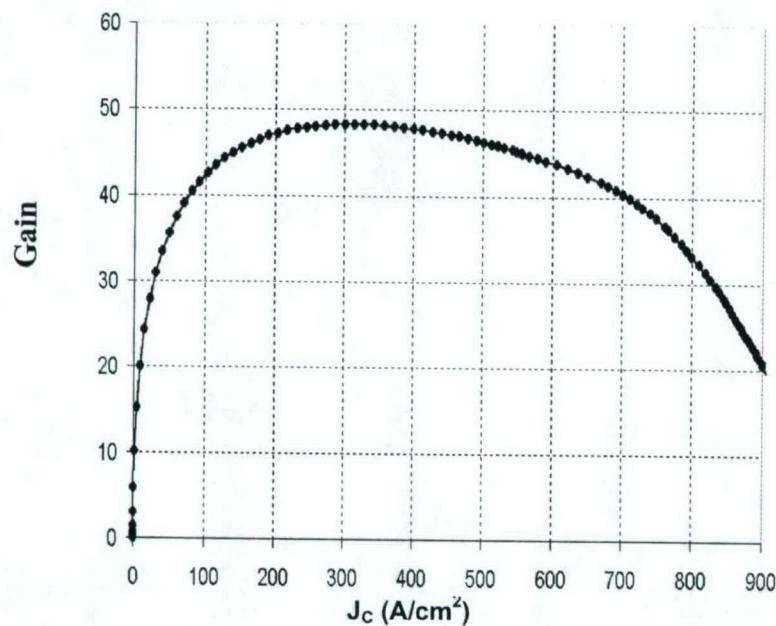


Fig. 10 Gain vs. J_c plot of the device in Fig. 8 ($V_{CE} = 10$ V).

2.2.3 5 kV Device performance at room temperature

Figure 11 shows on-state characteristics of a large device at room temperature. The device carries 1.2 A (115 A/cm^2) at a forward voltage of 11.5 V and base current of 80 mA. DC common emitter current gain is 15. The specific on-resistance is $78 \text{ m}\Omega \cdot \text{cm}^2$, about 1.9 times higher than the theoretical unipolar value for this epilayer. The higher resistance may be due to the long finger length, the variation of ρ_{cp} across the device, and relatively thin top metal. Figure 12 shows that BV_{CEO} is 3,200 V, about 40% of the theoretical value for this epilayer. The BV_{CEO} obtained here is limited by Tektronix 371A curve tracer. This device experienced a destructive breakdown at 3250 V in a later attempt to extract the breakdown voltage using a custom-made high voltage measurement system. The result is shown in Fig. 13. The leakage current density J_{CEO} is $6 \times 10^{-2} \text{ A/cm}^2$ at voltages below 2000 V, considering the area of the reverse biased P-N⁻ junction of the large BJT not including the JTE region. Notice that J_{CEO} is J_{CBO} amplified by current gain. J_{CBO} is around $4 \times 10^{-3} \text{ A/cm}^2$. The figure of merit $BV^2/R_{ON,SP}$ is 131 MW/cm², among the best reported SiC power devices.

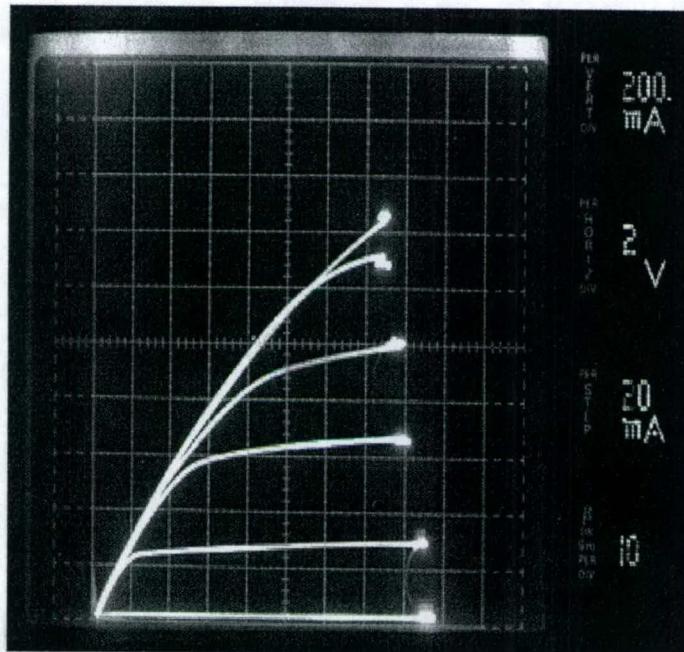


Fig. 11 I-V curve of a 5 kV device with active area 1.05 mm^2 (finger length = $350 \mu\text{m}$).

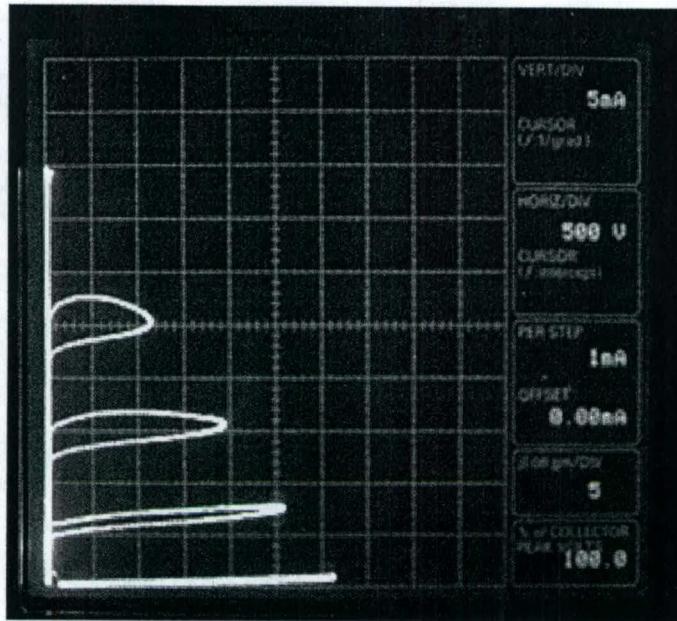


Fig. 12 The device in Fig. 11 shows BV_{CEO} around 3,200 V.

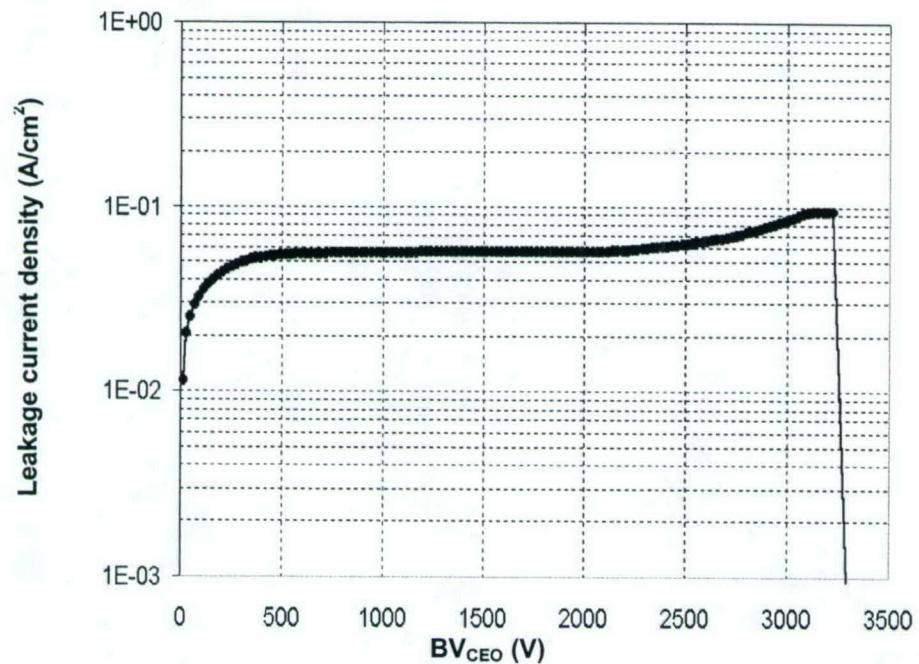


Fig. 13 Leakage current density vs. BV_{CEO} of the device in Fig 11.

Figures 14-16 show the on-state characteristics of a small BJT at room temperature. The device maintains a current gain greater than 20 up to collector current densities of $300 A/cm^2$ at $V_{CE} = 10 V$. The specific on-resistance $R_{ON,SP}$ obtained from Fig. 14 is $28 m\Omega \cdot cm^2$, smaller than

the theoretical unipolar value. From the Gummel plot, an ideality factor η_C close to 1 indicates that collector current is dominated by diffusion while base current is dominated by $2kT$ recombination current, which is consistent with 2 kV devices. The power dissipated in driving the base of the small BJT is only about 1.7 % of its total on-state power loss, assuming this device is driven at $V_{CE} = 10$ V, $J_C = 250$ A/cm². The corresponding current gain is 22.5.

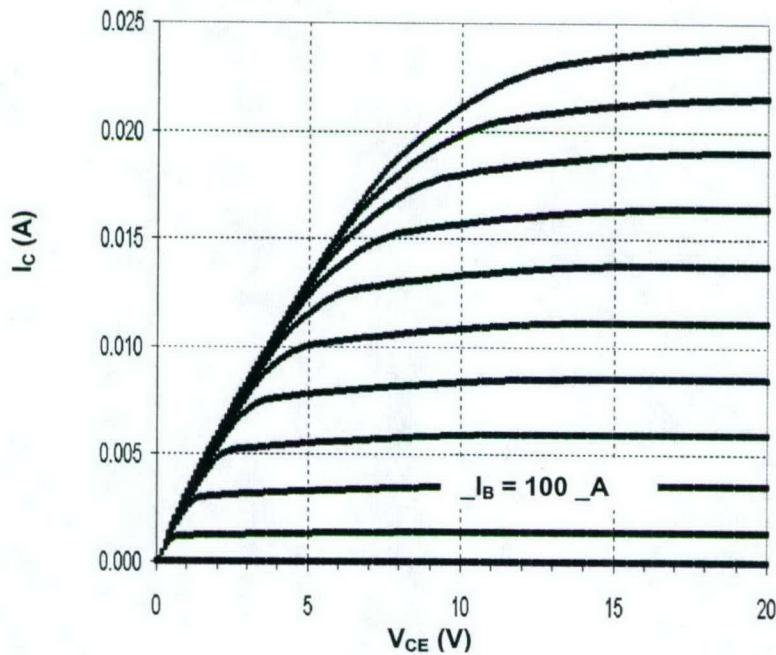


Fig. 14 I-V curve of a 5 kV device with active area 0.0072 mm^2
(finger length = $60 \mu\text{m}$).

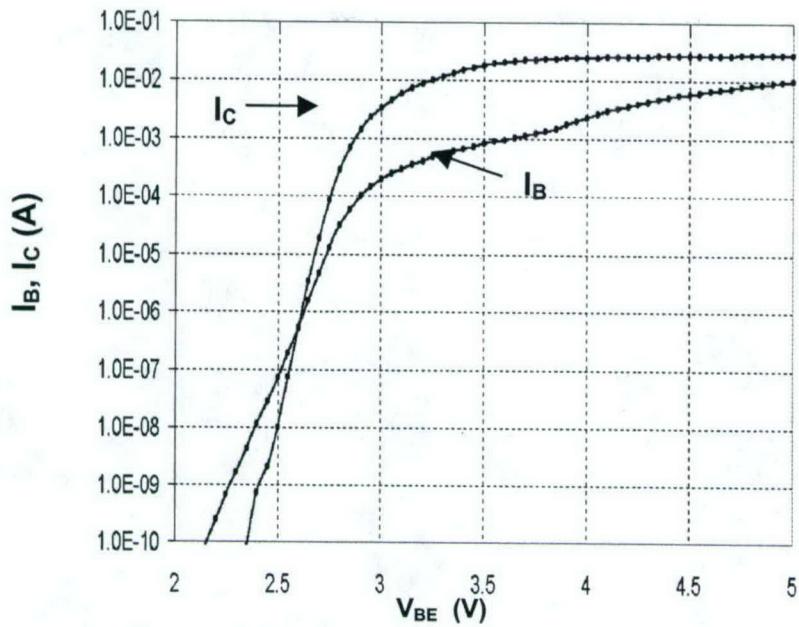


Fig. 15 Gummel plot of the device in Fig. 14 ($V_{CE} = 10$ V).

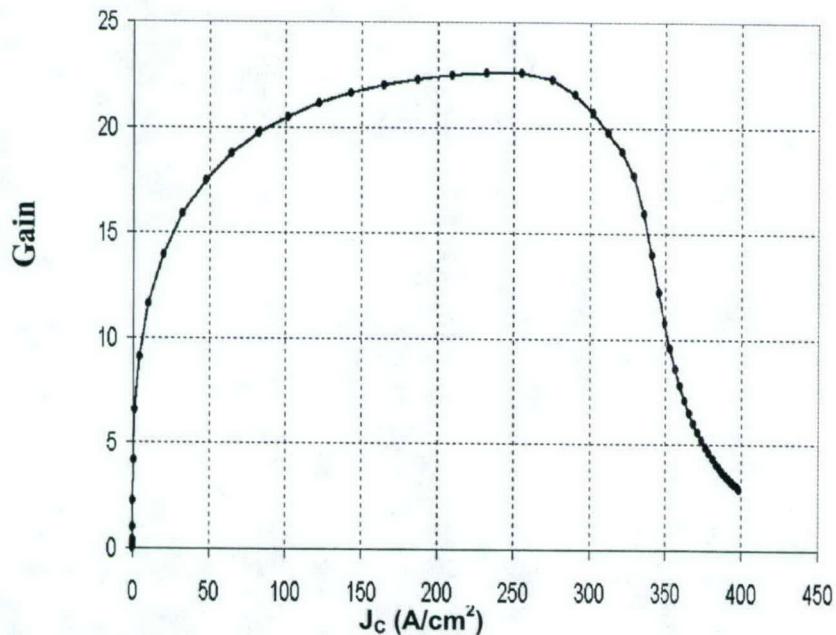


Fig. 16 Gain vs. J_c plot of the device in Fig. 14 ($V_{CE} = 10$ V).

2.2.4 Other important observations

The dependence of current gain on the spacing between the p+ base contact implant and the emitter edge is shown in Fig. 17 and 18a,b. It is clear from Fig. 17 that as the gap is narrowed, the ideality factors of both base and collector currents decrease to close to 2 and 1, and from Fig 18, as the p+ base contact implant is brought closer to the emitter edge, the current gain decreases monotonically. It is likely that the p+ base contact implant introduces defects into the SiC that are not completely removed during the implant activation anneal. As the defect sites are brought within one electron diffusion length from the emitter, they provide the recombination centers for laterally diffused electrons. This recombination process gives an excess component to the base current and degrades the ideality factor. As a consequence, the current gain is reduced. This concept is illustrated in Fig. 19.

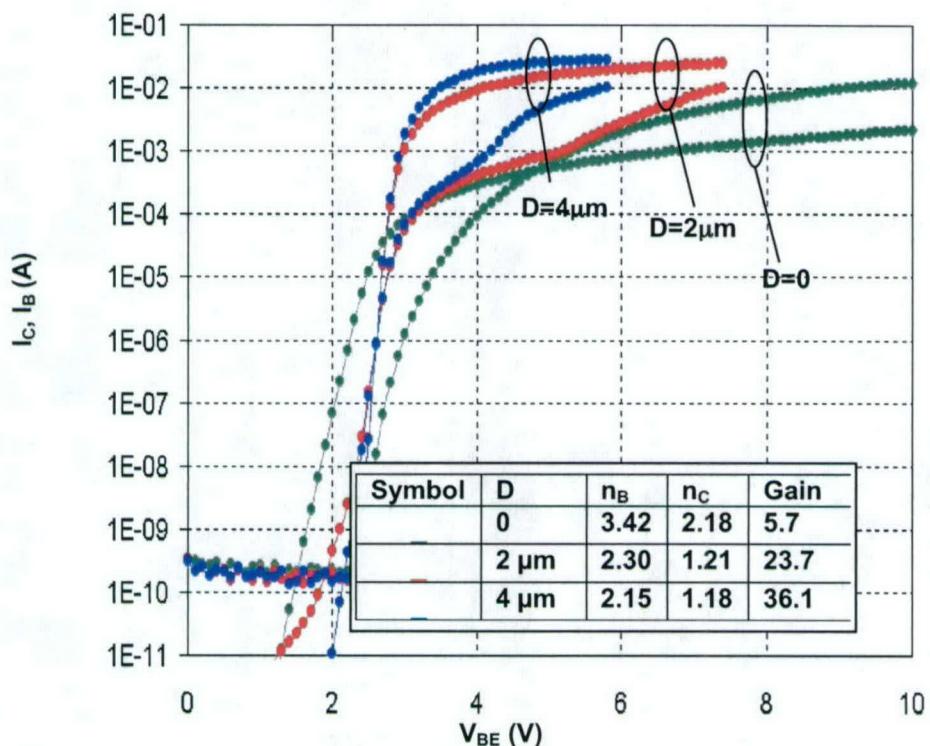


Fig. 17 Gummel plot of small 2 kV BJTs with different spacing between emitter and p+ implant ($V_{CE} = 10$ V).

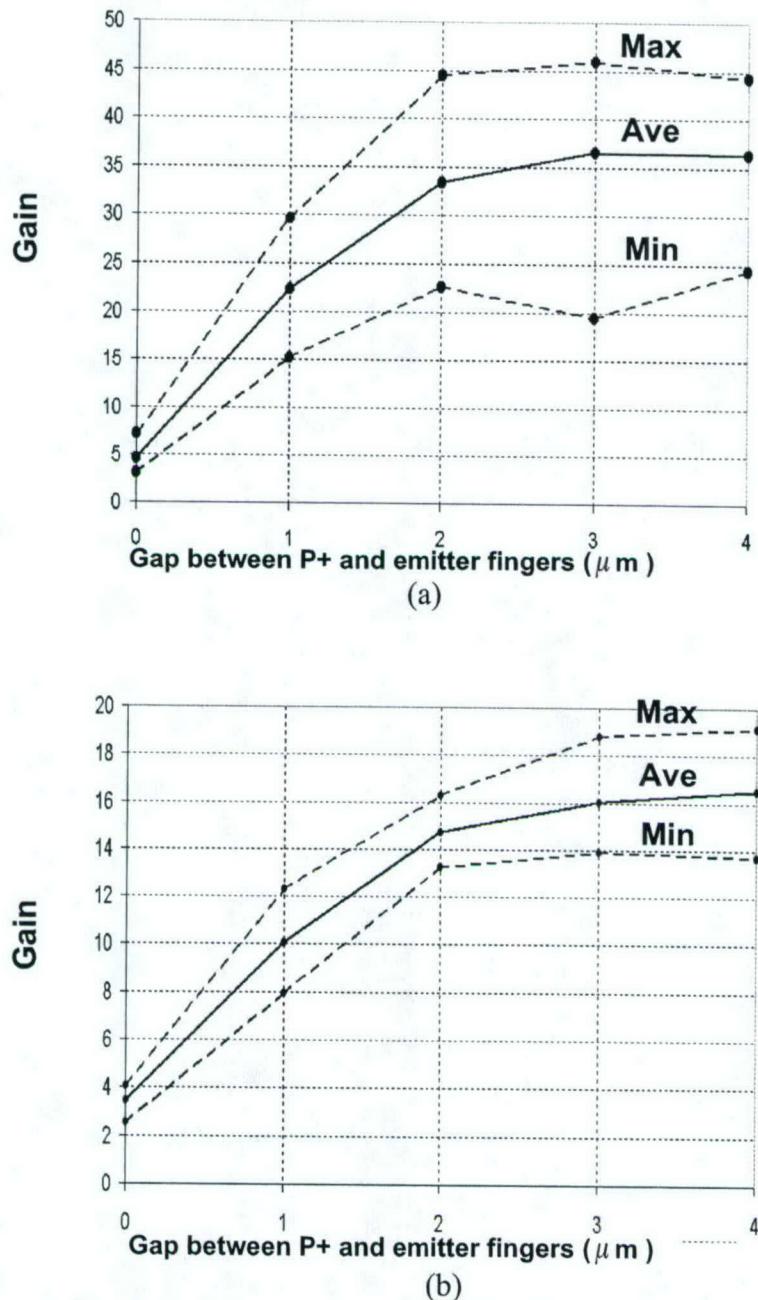


Fig. 18 Current gain of the BJTs as a function of spacing between the p-type base contact implant and the edge of the emitter: (a) 2 kV devices; (b) 5 kV devices.

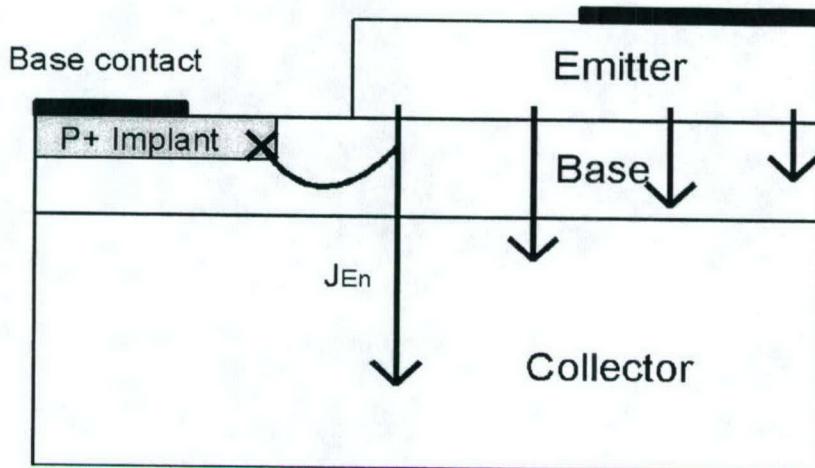


Fig. 19 Electrons recombine at implant-introduced defects.

Measurement results shown in Fig. 20a and 20b indicate a positive temperature coefficient of $R_{ON,SP}$ and a negative temperature coefficient of β , which is consistent with previous reports. The increasing resistance is believed mainly due to the reduction of carrier mobility at higher temperature. The decreasing current gain is mainly attributed to the increase of ionization percentage of aluminum acceptors in the base at higher temperature. However, we believe that R_{ON} also has a effect on the current gain at high temperatures, since the current density at the peak current gain is limited by R_{ON} , as mentioned in section 2.2.2. It can be observed from Fig. 21 that the current density at the peak gain decreases at higher temperature because of the strong temperature dependence of R_{ON} . And it can be extracted from Fig. 22 that the activation energy of current gain is around 65 meV at room temperature, much different from the aluminum acceptor energy. In general, it is believed that the observed high temperature performance makes the SiC BJT an attractive device for paralleling, since the current density will be reduced in the higher temperature device due to the decreasing current gain and increasing R_{ON} , which is a negative feedback.

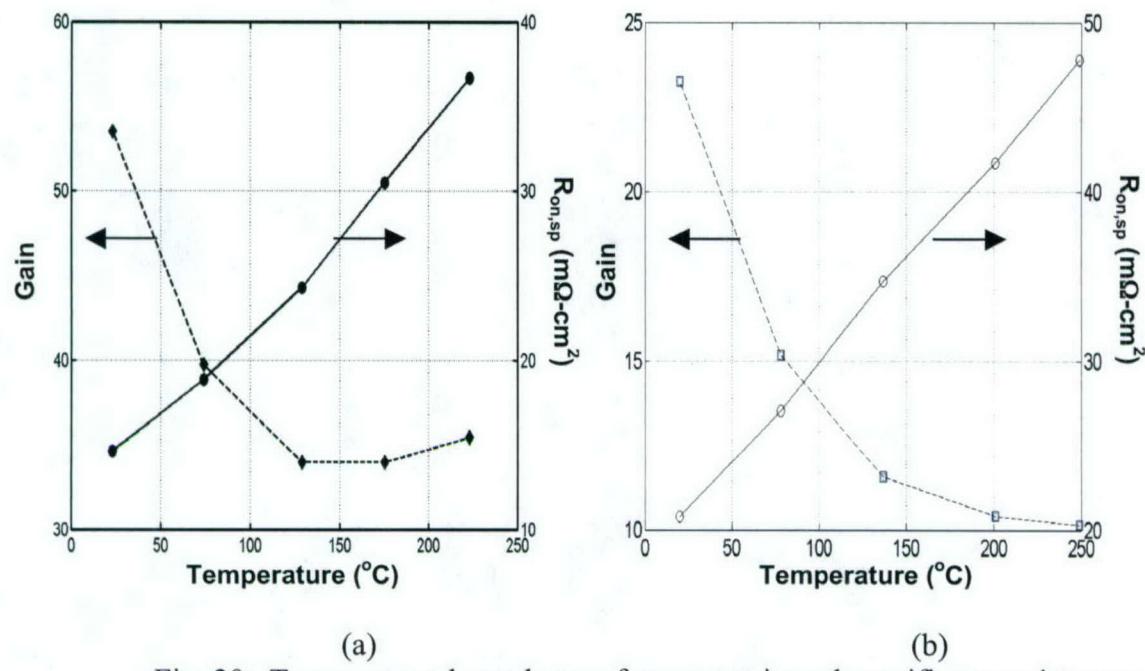


Fig. 20 Temperature dependence of current gain and specific on-resistance:
 (a) 2 kV large devices; (b) 5 kV small devices

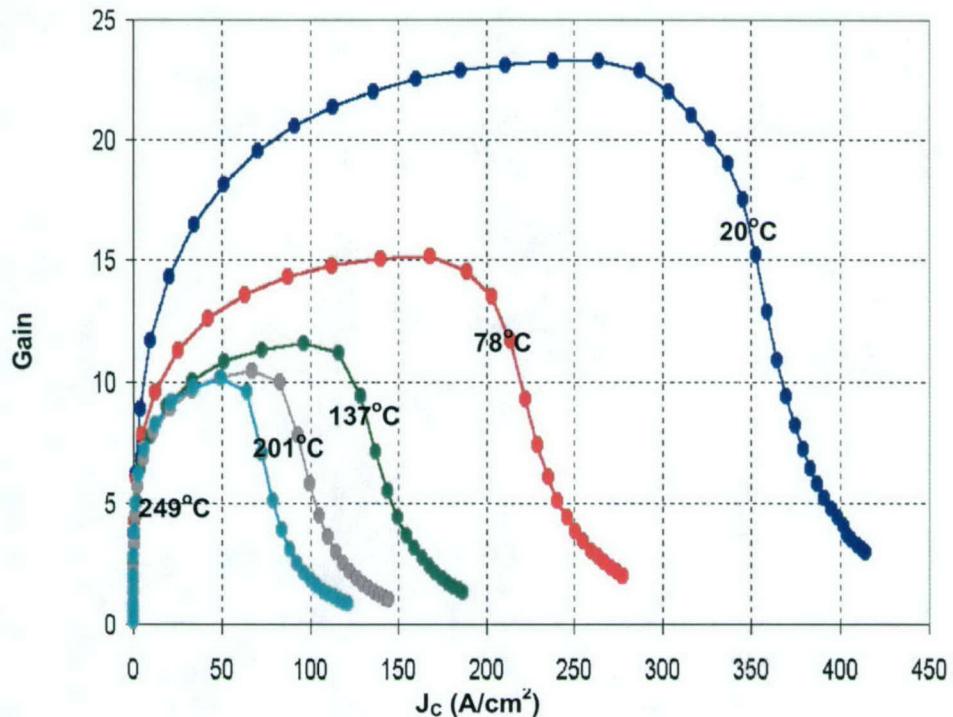


Fig. 21 Gain vs. J_C plot at different temperature for the 5 kV small devices ($V_{CE} = 10$ V).

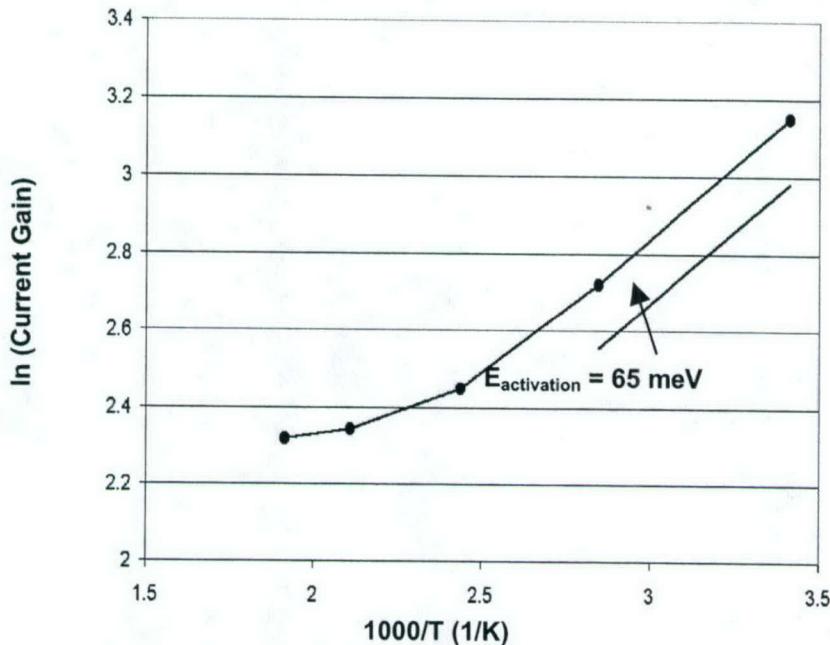


Fig. 22 Activation energy of current gain

When a SiC BJT is biased in its forward active state, the forward biased emitter-base junction will emit light due to radiative recombination of large number of excess carrier, though it is an inefficient recombination due to the indirect bandgap of SiC. And the excess carrier density is directly related to the current density. Based on the above reasoning, photographs are taken to see the current distribution in the device by observing the emitted light under bias. As shown in Fig 23a – d, in a small/short finger device, current flows relatively uniformly throughout the active area. However, in a large/long finger device, current is non-uniformly distributed due to non-uniform contact resistivity, especially in the base contact, as can be shown in Fig. 24. One of the possible reasons is that the aluminum based p-type contact metal is usually annealed beyond its melting point without enough capping material. During the anneal process the metal is melting and vaporizing, which makes the reaction between metal and semiconductor spatially non-uniform. Another possible reason is that there might be traces of oxygen leaking into the chamber and reacting with aluminum during the anneal. In order to get a larger current density in large BJT devices, contact uniformity needs to be further improved. The contact metal scheme should be re-examined.

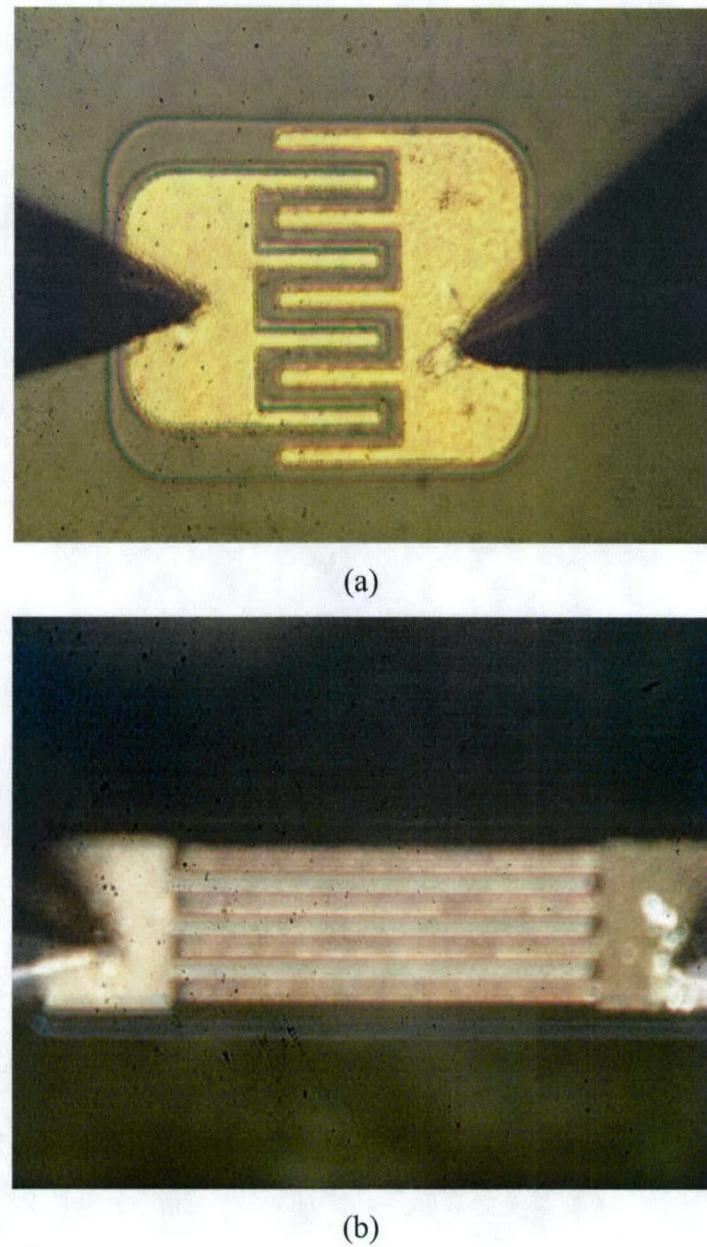
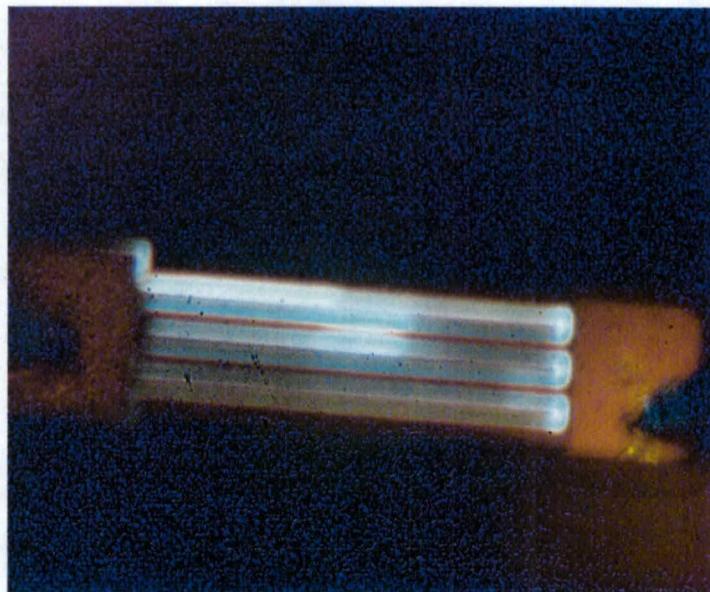


Fig. 23 Current distribution in BJTs in forward active mode: (a) a small device with $60 \mu\text{m}$ finger length; (b) a large device with $300 \mu\text{m}$ finger length.



(c)



(d)

Fig. 23 Current distribution in BJTs in forward active mode: (c) the small device under bias;
(d) the large device under bias.

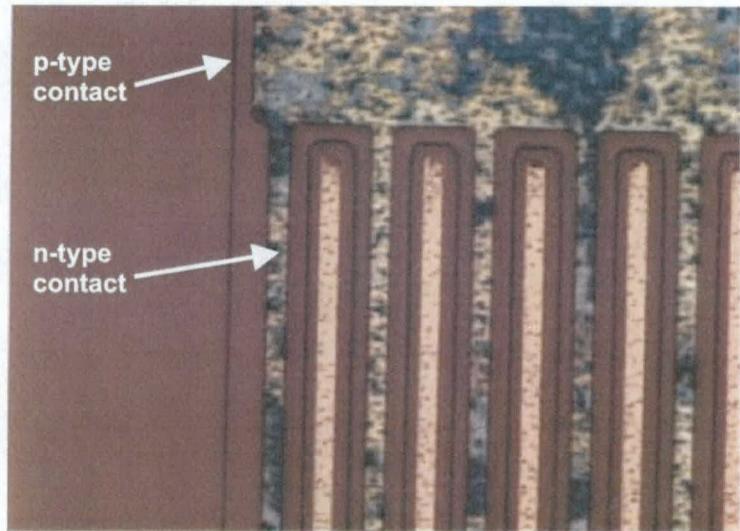


Fig. 24 Photomicrograph of annealed p-type and n-type contacts. p-type contact morphology is non-uniform.

3. Fabrication and Experimental Results on the “Production” Wafers (*Wafers #1 – 6*)

This section discusses the design, fabrication, and experimental results of the “production” wafers (*Wafers #1–6*). To produce as many BJTs and PiN diodes as possible within a 50 mm wafer, all devices are optimized to block 2 kV, and all devices utilize the fabrication procedures and layouts developed on “test” Wafer #0. In the “production” wafers, the spacing between the p+ base contact implant and the edge of the emitter fingers is set at 4 μm . No PiN diodes are included in the “production” wafers, but any BJT that does not exhibit a minimum acceptable current gain (typically $\beta \geq 8$) but still has $\text{BV} \geq 1,000 \text{ V}$ is used as PiN diodes by shorting the emitter to base.

3.1 Design and Fabrication of “Production” 4H-SiC BJT Wafers #1 – 3

The overall dimensions of the “production” BJTs are illustrated in Fig. 25. The entire 50 mm wafer is covered with this pattern, except for 12 test sites. This provides a total of 303 BJT

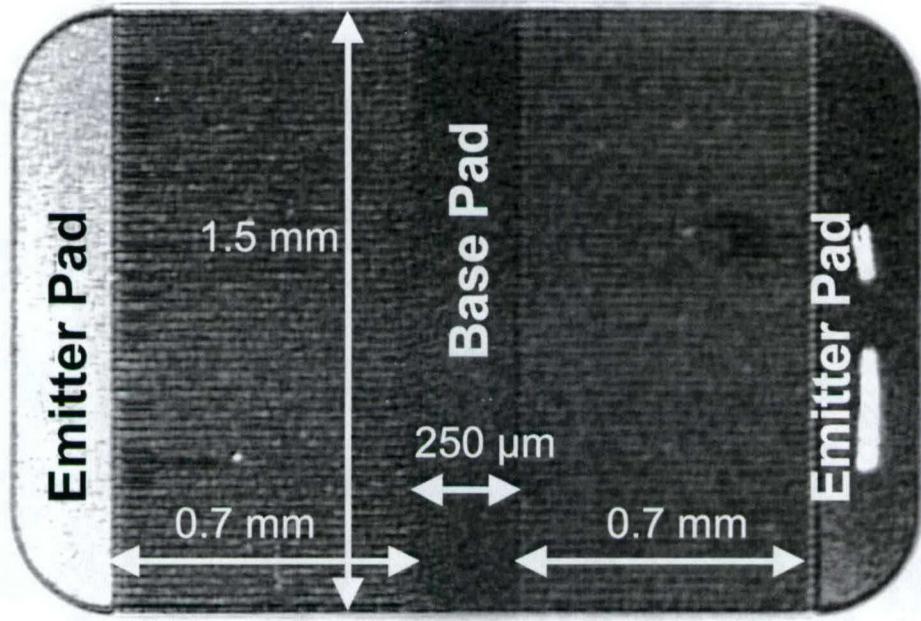


Fig. 25. Layout dimensions of the “production” 2 kV BJTs. The active area of the interdigitated emitter-base fingers is 0.021 cm^2 . At a current density of 100 A/cm^2 , this device would carry approximately 2 A.

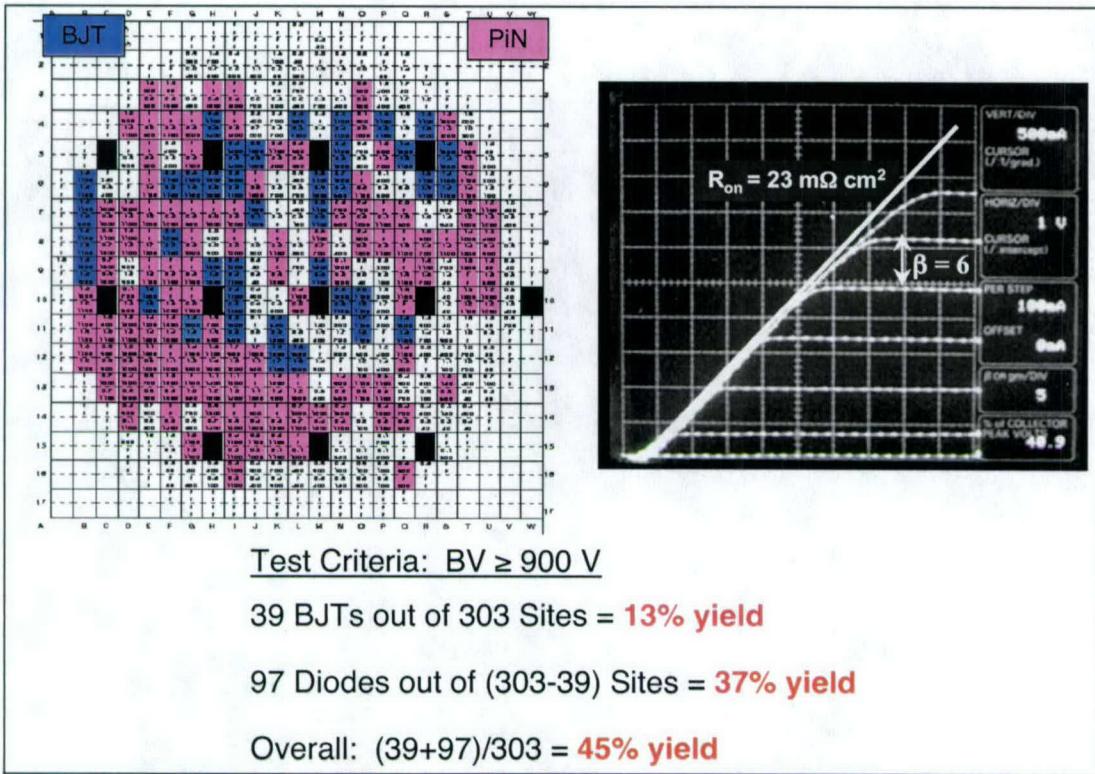


Fig. 26. Wafer map, on-state characteristics, and yield statistics for BJT Wafer #1. Blue sites in the wafer map correspond to 39 BJTs with $\beta > 6$ and $BV \geq 900$ V. The purple sites correspond to BJTs with $\beta < 6$ but $BV \geq 900$ V. These purple devices are used as PiN diodes. The on-state characteristics shown here are measured on *one-half* of an active device, with active area of 0.01 cm^2 .

sites on a 50 mm wafer.

Figure 26 shows a wafer map and associated yield statistics for BJT Wafer #1. Current gain was low for this wafer, and a minimum beta of 6 was selected as the criterion for use as a BJT. This resulted in 39 BJTs and another 97 PiN diodes, all of which blocked ≥ 900 V. As seen in the figure, one half of the BJT carried 3.5 A at a forward voltage drop of 7.5 V, for a specific on-resistance of about $23 \text{ m}\Omega \text{ cm}^2$.

After the wafer was diced for packaging, a problem developed during packaging: the aluminum top metal peeled off during wire bonding. The problem was traced to the photoresist developer, AZ4620, that was used for Ni liftoff during formation of the emitter ohmic contacts. The developer attacked the Ni underlying the top Al layer, causing the metal to swell and

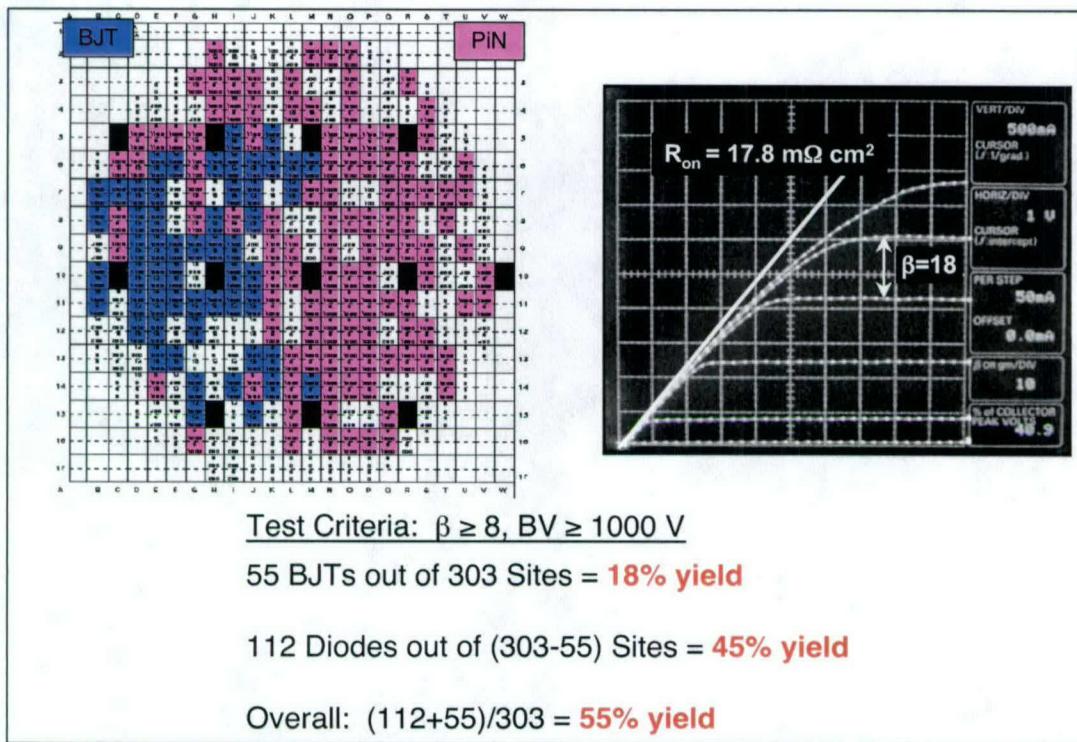


Fig. 27. Wafer map, on-state characteristics, and yield statistics for BJT Wafer #2. Blue sites in the wafer map correspond to 39 BJTs with beta ≥ 8 and BV $\geq 1,000$ V. The purple sites correspond to BJTs with beta < 8 but BV $\geq 1,000$ V. These purple devices are used as PiN diodes.

degrading adhesion. This problem was solved in subsequent runs by switching to a different developer, AZ1516, but since Wafer #1 had already been diced, it was not possible to reprocess this wafer. As a result, we did not get any packaged devices from the first processing run.

Figures 27 and 28 show the wafer maps and yield statistics for BJT Wafers #2 and #3, respectively. Wafers #2 and #3 exhibited slightly higher gain and blocking voltage than Wafer #1, and the yield criteria for these two wafers are beta ≥ 8 and BV $\geq 1,000$ V. Wafer #2 yielded 55 BJTs and 112 PiN diodes, while Wafer #3 yielded another 54 BJTs and 86 PiN diodes. This represents a total of 109 BJTs and 197 PiN diodes from the two wafers, with a BJT yield of 18 % on each wafer and a PiN diode yield of 45 and 35 %, respectively. Specific on-resistances are approximately 18 and 22 $m\Omega \text{ cm}^2$ for the two wafers. These resistances are expected to be lower after the devices are packaged, since the absolute on-current of 2-3 A passing through a single

probe tip during wafer probing will produce a significant voltage drop, but this drop should be

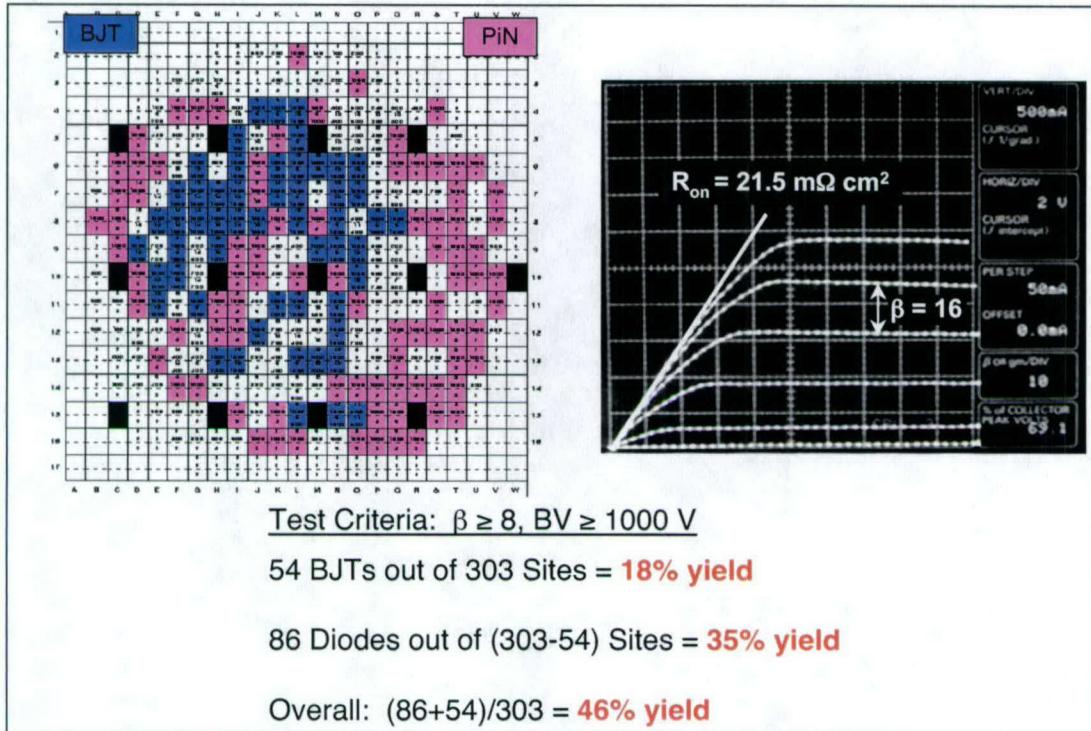


Fig. 28. Wafer map, on-state characteristics, and yield statistics for BJT Wafer #3. Blue sites in the wafer map correspond to 39 BJTs with $\beta \geq 8$ and $BV \geq 1,000$ V. The purple sites correspond to BJTs with $\beta < 8$ but $BV \geq 1,000$ V. These purple devices are used as PiN diodes.

minimized when the current is distributed among multiple wire bonds in the packaged parts.

In order to test the viability of the new metal processing, Wafer #3 was cut into quarters, and one quarter was diced. The remaining quarters of Wafer #3 and all of Wafer #2 were not diced, so that these wafers could be reprocessed if the packaging test revealed problems with the metallization scheme. During package testing with die from Wafer #3 at PowerEx, the backside metal peeled off during die attach. The die were eventually mounted in the packages with conductive epoxy, and wire bonding to the test die was successful. Figure 29 shows photographs of packaged test BJTs from the diced quarter of Wafer #3.

Following these bonding tests, Wafer #2 and the remaining three quarters of Wafer #3 were diced and sent to PowerEx for bonding. Unfortunately, problems were encountered with top metal peeling during bonding, such that the yield of packaged devices was very low. At this

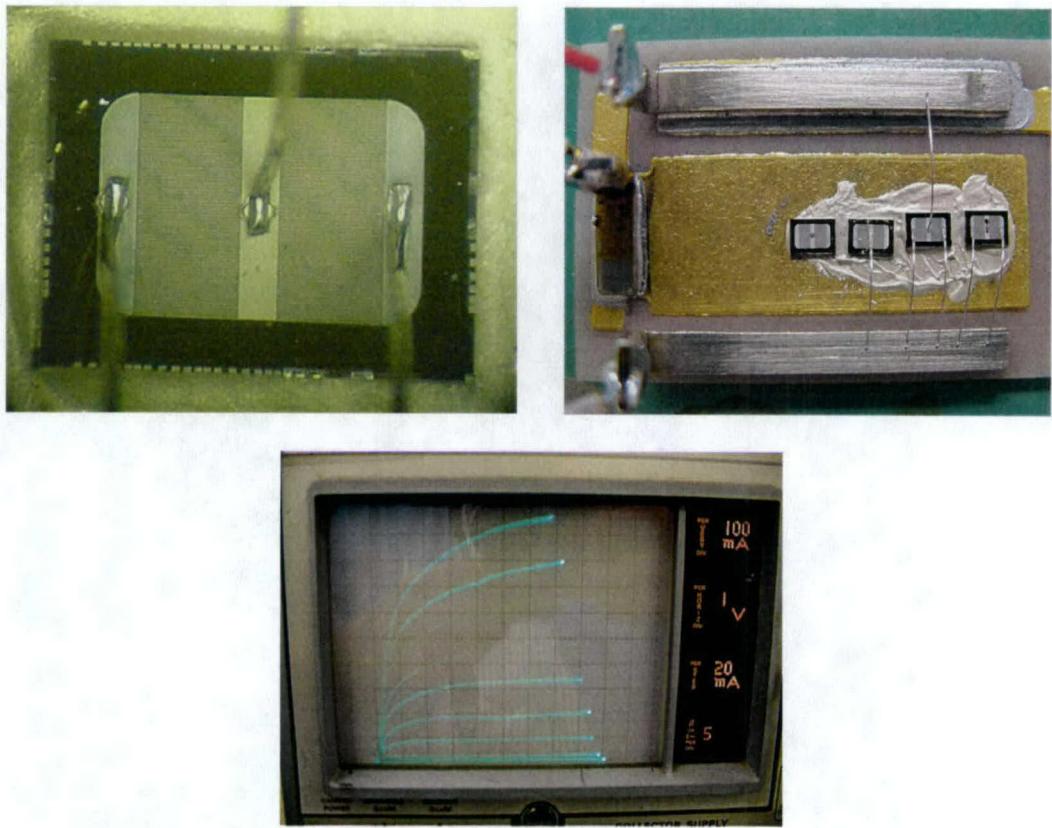


Fig. 29. BJTs from Wafer #3, mounted with conductive epoxy and wire bonded at PowerEx. The on-state operation of a packaged BJT is also shown.

point, we halted further production of BJTs and concentrated on solving the metal adhesion problem.

3.2 Modifications to the Metallization Scheme to Improve Wire Bond Adhesion

The poor adhesion of wire bonds to the top metal of the emitter and base contact pads are believed caused by a carbon-rich layer that develops on the top surface of the ohmic contact metal during contact annealing. During the annealing process, Ni ohmic contacts form a Ni-silicide alloy that releases carbon from the SiC lattice, and several reports indicate that this carbon accumulates on the Ni surface. If this carbon-rich layer is not removed prior to deposition of the thick top metal (typically Ti-Al or Ti-Au), the top layer will not adhere to the carbon-rich layer, and will peel during wire bonding. We were able to eliminate this problem by

introducing a rigorous cleaning procedure at two points in the process: (i) before deposition of the ohmic metal layer, and (ii) after ohmic contact anneal but prior to deposition of the thick top metal layer. The full procedure for the P+ ohmic contact and top bonding pad metal is detailed below:

1. P+ Liftoff Lithography: Deposit, expose, and develop photoresist.
2. RIE in SF₆ at 100 W for 1 min (removes organic residue from the PR)
3. Barrel etch in O₂ plasma at 100 w for 2 min (removes flourinated hydrocarbon residue from the RIE step)
4. Dip in BHF for 20 sec (removes oxide layer formed during plasma etch)
5. Deposit P+ Ohmic Contact Metal (0.2 μ m, 75/25 wt. % Ti/Al) using e-beam evaporation at base pressure $\leq 5 \times 10^{-7}$ Torr
6. Lift Off P+ Contact Metal
7. Soak in acetone for 1 hour and methanol for 1 hour
8. Perform contact anneal in vacuum at 1000 °C for 2 min
9. Barrel etch in O₂ plasma at 100 W for 1 min (removes metallic contaminants from annealing chamber)
10. Dip in BHF for 20 sec (removes oxide layer formed during plasma etch)
11. P+ Top Metal Liftoff Lithography: Deposit, expose and develop photoresist.
12. RIE in SF₆ at 100 W for 1 min (removes organic residue from the PR)
13. Barrel etch in O₂ plasma at 100 w for 2 min (removes flourinated hydrocarbon residue from the RIE step)
14. Dip in BHF for 20 sec (removes oxide layer formed during plasma etch)
15. Deposit Top Metal (1.7 μ m Au on base fingers, 3.1 μ m Au on bonding pads)
16. Liftoff Top Metal

A similar procedure is used for the N+ ohmic contact to the emitter, except that the ohmic metal in step 5 is 70 nm of Ni. It is found that the sequence: RIE-Barrel Etch-BHF prior to deposition of ohmic metals (steps 2 – 4) and prior to deposition of top metal (steps 12 – 14) successfully eliminates the adhesion problem. To further insure that no carbon residue is present under the

top metal bonding pads, we modified the mask set to remove the ohmic contact metals in the large-area bonding pad regions, leaving ohmic contact metal only along the interdigitated fingers. This places the top metal in the large bonding pad areas on an oxide layer, further promoting adhesion. These modifications were put into place for Wafers 4 – 6.

Back-side metal adhesion was improved using the same RIE-Barrel Etch-BHF sequence as the top metal, both before ohmic metal deposition, and after ohmic contact anneal but before top metal deposition. In addition, we used a 48 nm/15 nm Ni/Cr metal stack on the back side, since reports from John William's group at Auburn University indicate that the Ni/Cr stack minimizes carbon segregation upon contact annealing. The revised back-side contact procedure was successful in preventing back-side metal peeling during die attach. All these improvements were incorporated into the fabrication sequence for the last three wafers, #4, #5, and #6.

3.3 Fabrication of “Production” 4H-SiC BJT Wafers #4 – 6

The processing of Wafers 4 – 6 encountered unexpected problems with ohmic contact, which was later determined to be due to contaminated metal in the new CHA e-beam evaporator. This resulted in non-ohmic contacts on all three wafers. In an attempt to isolate the problem, Wafer #4 was cut in half, and one half cut into quarters. This quarter-wafer was reprocessed by etching all ohmic metals and all passivation oxides. A new passivation oxide was deposited using the Lindberg oxidation furnace, a system usually used for sacrificial oxides. This was done to avoid contamination of our clean MOS oxidation tubes by inserting a wafer that had once had metals. The re-worked quarter-wafer of Wafer #4 was given new ohmic metals using the Varian e-beam evaporator, and the resulting ohmic contacts were acceptable: P+ contacts had resistivities of $1.2 - 6.5 \times 10^{-2} \Omega \text{ cm}^2$ and N+ contacts had resistivities of $1.6 - 8.4 \times 10^{-5} \Omega \text{ cm}^2$ after top metal. Typical current gains were about 9, and BV_{CEO} was over 1,000 V. Figure 30 shows a wafer map of this quarter-wafer after reprocessing. The yields are lower than for Wafers 1 – 3, due to the extensive reprocessing of this wafer. The beta is also lower, probably due to the use of a low-quality passivation oxide necessitated by the reprocessing. This quarter-wafer has been sent to Cree, Inc. for dicing. Dr. Anant Agarwal of Cree has graciously agreed to package the viable BJTs and diodes from this quarter-wafer in TO-219 for us.

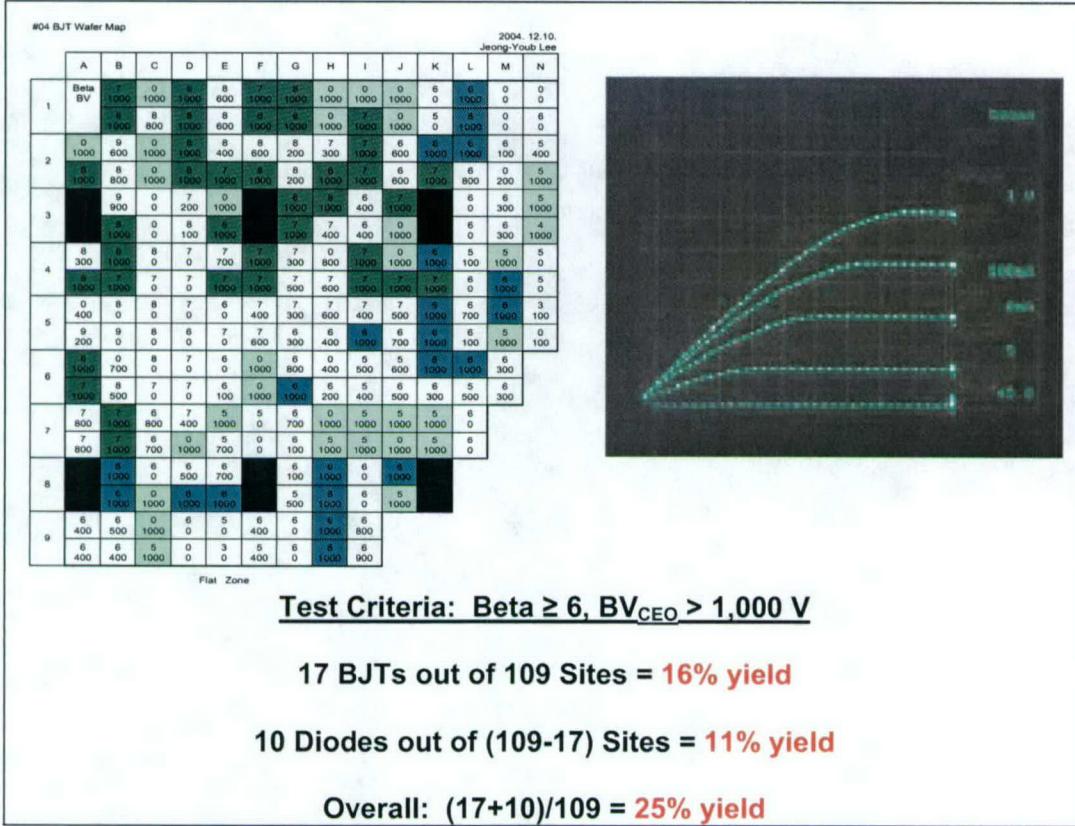


Fig. 30. Wafer map, on-state characteristics, and yield statistics for a quarter-wafer of BJT Wafer #4. Blue sites in the wafer map correspond to 12 BJTs with beta ≥ 7 and BV_{CEO} $\geq 1,000$ V. Dark green sites correspond to 5 BJTs with beta = 6 and BV_{CEO} $> 1,000$ V. Light green sites correspond to 10 BJTs with beta < 6 but BV $\geq 1,000$ V. These light green devices are used as PiN diodes.

Wafers #5 and #6 are currently being reprocessed in the same manner as Wafer #4, since they also suffered from the metallization problem caused by the contaminated metal in the CHA e-beam evaporator. It is our intention to complete these two wafers, have them diced, and have BJTs and PiN diodes packaged and transferred to the Purdue power systems group under Prof. Scott Sudhoff for evaluation in their motor control breadboard.

The next section describes the development and testing of the motor control system breadboard using silicon BJTs and diodes.

4. Development and Testing of an Induction Machine Drive for Use with SiC BJTs and PiN Diodes

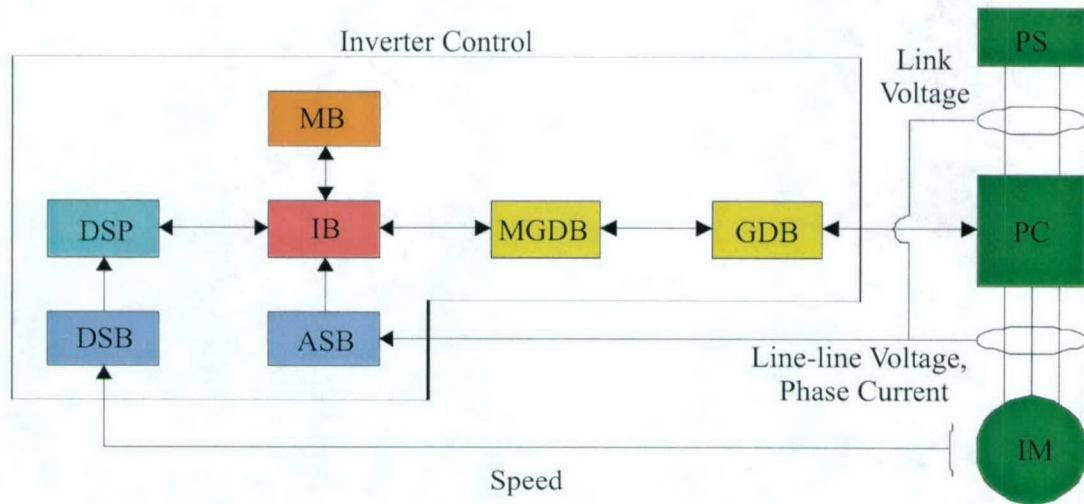
C. Kwon, S.F. Glover, S.D. Sudhoff
Purdue University

4.1 Overview

For the purpose of demonstrating the SiC based power semiconductor devices, BJTs and diodes fabricated in SiC are being applied in the context of a fully functional power electronic converter application. For this demonstration, a 4 kW motor drive has been constructed as a test bed. In this report, the motor drive will be explained and its performance reported. In this drive, Si BJTs and diodes are currently used but will be replaced with SiC devices when they become available.

The drive block diagram is illustrated in Fig. 31. The drive is designed to be used with a 4 kW Induction Machine (IM) and have a dc rail voltage up to 400 V dc. The Power Converter (PC) is an inverter whose topology is shown in Fig. 32. The inverter is comprised of six sets of paralleled BJTs (modest design changes should allow operation of 1 kV) which is provided by the Power Supply (PS) and one anti-parallel diode which are labeled T1 – T6. A hysteresis brake type dynamometer is used to load the induction machine (Magnetek 6-850176-01-00).

The Inverter Control which determines the switching command signals to the power semiconductor devices consists of seven blocks. These include Digital Signal Processor (DSP) block, Digital Sensor Board (DSB), Analog Sensor Board (ASB), Modulator Board (MB), Interface Board (IB), Master Gate Drive Board (MGDB), and Gate Drive Board (GDB). A description of each block will follow.



MB=Modulator Board

DSP=Digital Signal Processor

IB=Interface Board

MGDB=Master Gate Drive Board

DSB=Digital Sensor Board

PS=DC Power Supply

GDB=Gate Drive Board(s)

PC=Power Converter (Inverter)

IM=Induction Machine

ASB=Analog Sensor Board

Fig. 31 The configuration of the test bed constructed

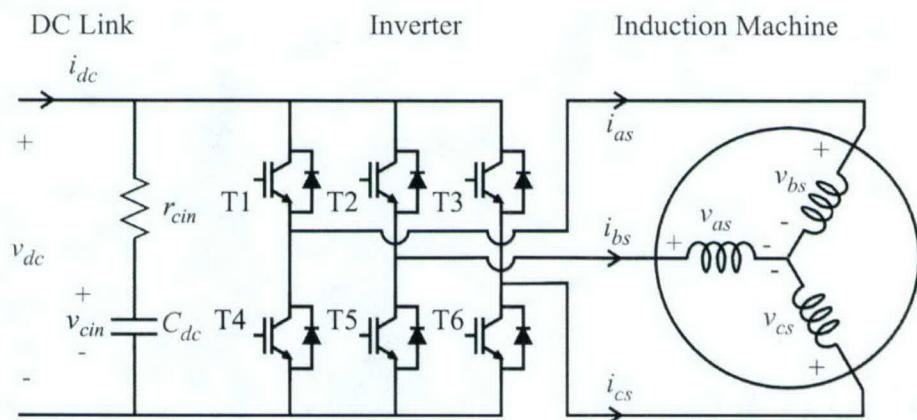


Fig. 32 The Power Electronic Converter Topology for the test bed

4.2 Detailed Description of Circuit Blocks

4.2.1 Digital Signal Processor (DSP)

This block generates *abc*-phase inverter current commands, $\mathbf{i}_{abc}^* = [i_{ai}^* \ i_{bi}^* \ i_{ci}^*]$ to the modulator board wherein a vector of base switching command signal $\mathbf{s}_{abc}^* = [s_a^* \ s_b^* \ s_c^*]$ will be determined. Therein, for a given commanded torque T_e^* , a maximum torque per amp (MTPA) control strategy determines the inverter current command in the synchronous reference frame as well as a slip frequency command, which are denoted $\mathbf{i}_{dqi}^{e*} = [i_{qi}^{e*} \ i_{di}^{e*}]$ and ω_s^* , respectively. The synchronous current regulator (SCR) is used to ensure that the commanded currents are obtained. Therein, the measured *a*- and *b*- phase inverter currents, \hat{i}_{ai} and \hat{i}_{bi} , from Analog Sensor Board (ASB) are transformed to the synchronous reference frame and used to generate the error between the actual and commanded *q*- and *d*- axis currents. This error is multiplied by the integral gain, integrated, limited, and added back to \mathbf{i}_{dqi}^{e*} . The modified *q*- and *d*- axis current commands are transferred back to *abc* variables. The electrical frequency which is sum of the electrical rotor frequency, ω_r , and slip frequency command is integrated to determine the position of the synchronous reference frame θ_e . This procedure is depicted in Fig. 33. The control is implemented using an M44 DSP development package by Innovative Integration.

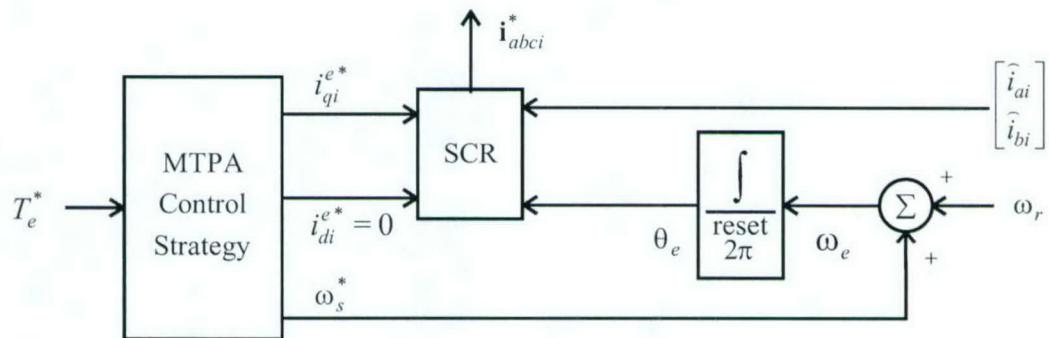


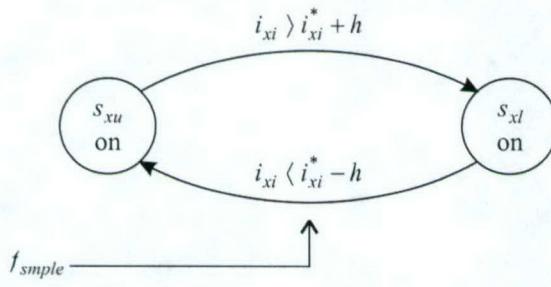
Fig. 33. Procedure implemented in Digital Signal Processor

4.2.2 Sensor Boards

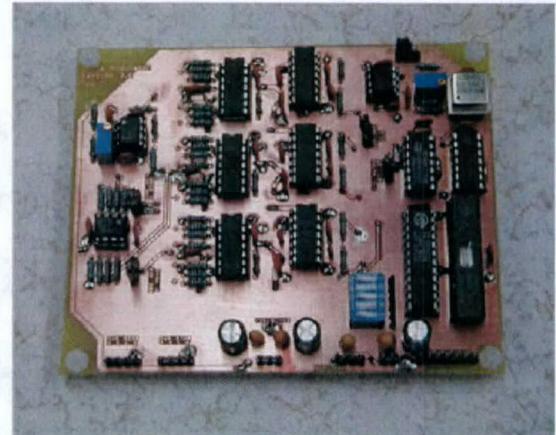
The test bed constructed utilizes two sensor boards. One board, which is Analog Sensor Board and labeled ASB in Fig. 31, senses *a*- and *b*- phase inverter currents, \hat{v}_{abi} and \hat{v}_{bci} , from inverter current sensors and two line-to-line inverter voltages, from inverter voltage sensors. The other board, which is Digital Sensor Board and labeled DSB in Fig. 31, senses induction machine rotor velocity to provide the number of pulses per revolution through an encoder.

4.2.3 Modulator Board

The Modulator Board generates a vector of base switching command signal $\mathbf{s}_{abc}^* = [s_a^* \ s_b^* \ s_c^*]$ for the power semiconductor switching devices in converter phase legs. Herein, hysteretic-delta (H-D) modulation is used. On every rising edge of the clock with frequency f_{sample} of 60 kHz, the *x*-phase inverter current command i_{xi}^* is compared to the actual current, i_{xi} , adjusted by the hysteresis level, h , which is 1 A in this work. The result of the comparison determines the commanded state for the phase leg. The switching of the three phases is staggered in time in order to minimize electromagnetic interference (EMI). Fig. 34 depicts a state transition diagram for one phase leg of the H-D modulator and its hardware implementation in board.



(a) The state transition diagram for one phase leg



(b) The hardware implementation

Fig. 34. H-D Modulator

4.2.4 Interface Board

This Interface Board buffers and filters the analog signals from the Analog Sensor Board and prepares the signals for A/D conversion. The first part of the board optically isolates signals from the Analog Sensor Board. Since the DSP sampling frequency is less than 10 kHz and the bandwidth of the measured quantities is larger than 10 kHz, an anti-aliasing filter is used to condition the signals. The second part of the Interface Board is to transfer a vector of base switching command signal $s_{abc}^* = [s_a^* \ s_b^* \ s_c^*]$ for the power semiconductor switching devices to Master Gate Drive Board. Fig. 35 illustrates the hardware implementation of Interface Board.

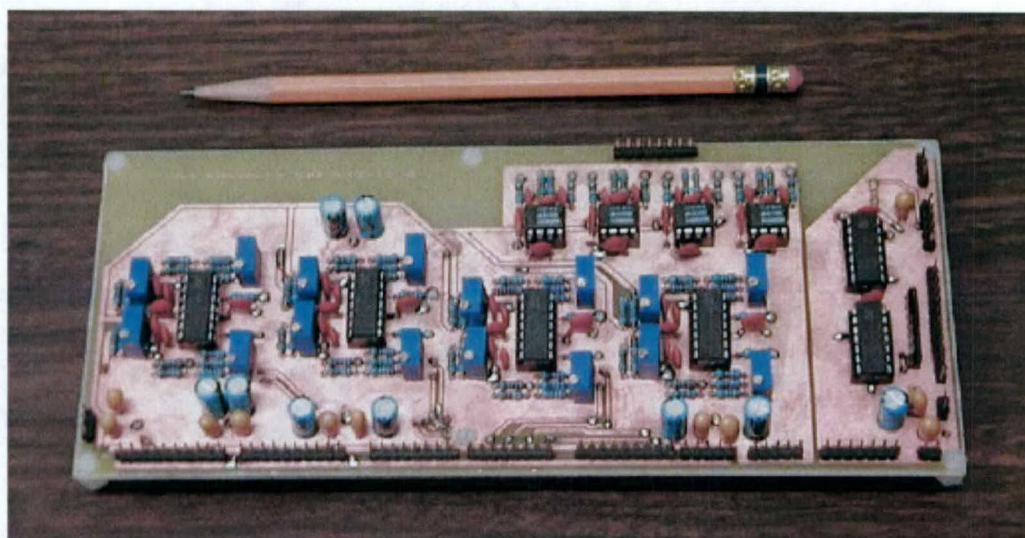


Fig. 35. Hardware implementation of Interface Board

4.2.5 Master Gate Drive Board

The function of the Master Gate Drive Board is to allow the operator to control the inverter while at the same time providing safeguards to protect the converter from potentially damaging overcurrents in the power semiconductor devices. This board also provides manual switches to allow the operator to disable individual power semiconductor devices. The hardware implementation is shown in Fig. 36.

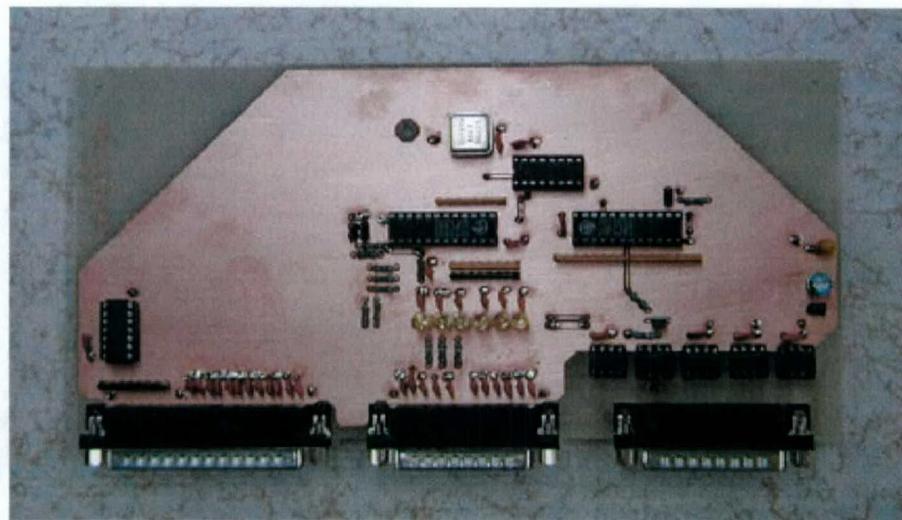


Fig. 36. Hardware implementation of Master Gate Drive Board

4.2.6 Gate Drive Board

The main functions of the Gate Drive Board are i) to turn on and off each BJT depending on the switching command signal to each power semiconductor device which is generated by the hysteretic delta (H-D) modulator, and ii) to generate a fault signal in the event of a short circuit during operation to protect power switching devices. To protect power semiconductor devices, overcurrent detection circuit is included. To enhance the switching characteristics, totem-pole base current control is utilized. Fig. 37 illustrates the block diagram of the Gate Drive Board. This board is composed of two power supplies and a switching control unit.

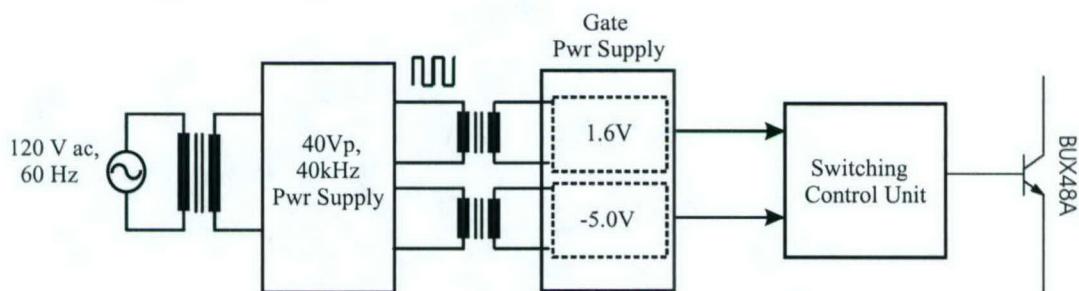
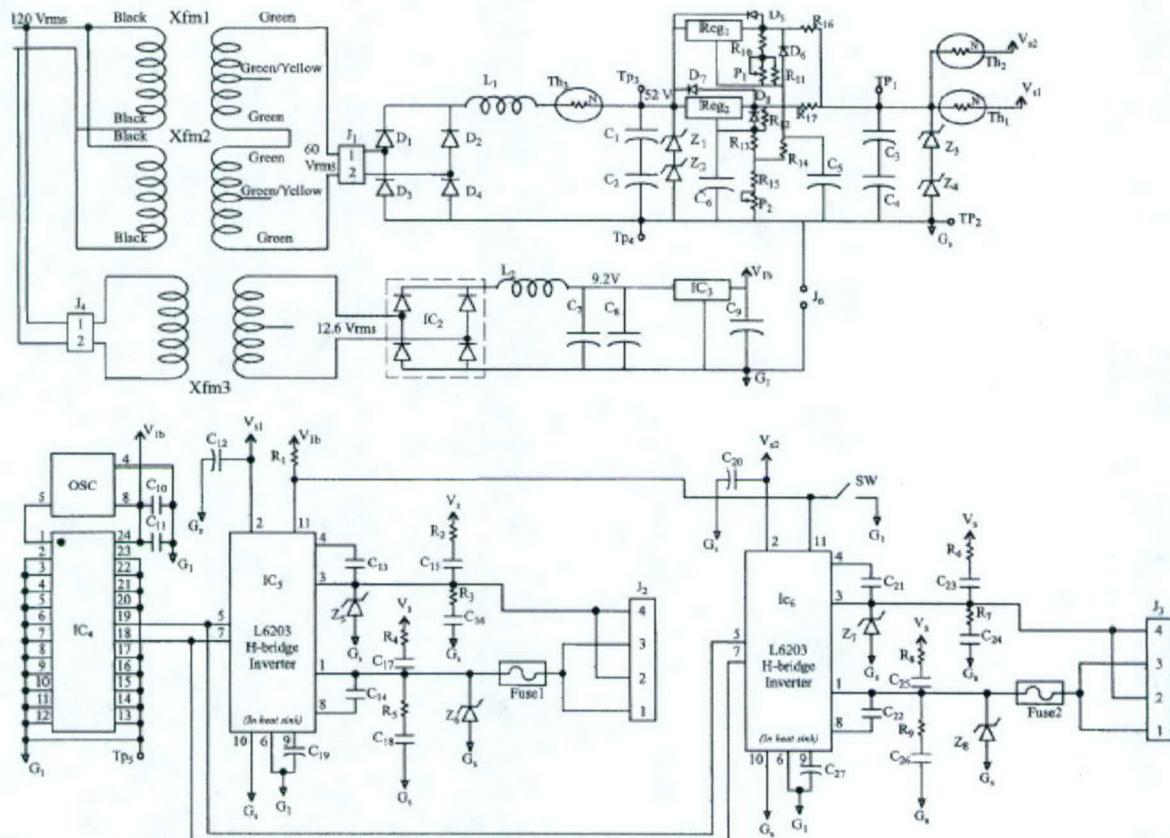


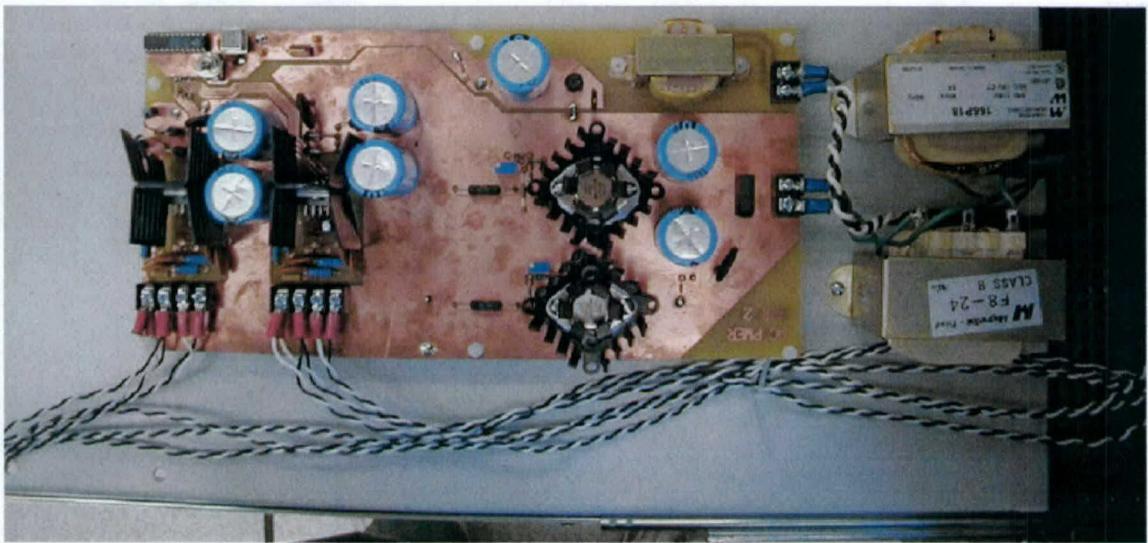
Fig. 37. The block diagram of Gate Drive Board

4.2.6.1 Square Wave Power Supply

This power supply generates 40 Vp, 40 kHz square waveform which will be stepped down and rectified to 1.6 V dc and -5 V dc to control the base of BJT. The power supply utilizes 120 V ac for its input power. This voltage is first stepped down to 60 Vrms and 12.6 Vrms through transformers. The 12.6 Vrms is necessary to provide 5 V to other logic devices on the same board. The 60 Vrms is rectified using a full-wave diode rectifier. The rectified voltage is regulated using two 3-terminal 5A adjustable voltage regulators. This provides up to 10 A at around 40V dc. Finally, the 40 Vp, 40 kHz square waveform at the output is generated through a full bridge inverter. In this test bed, L6203 H-bridge inverter by STMicroelectronics is used. This high frequency voltage output is used as the power source by the gate drive circuits. The use of high frequency reduces the size of the gate drive power supply transformers. The block diagram of the square wave power supply and the hardware implementation of this power supply are shown in Fig. 38.



(a) Schematic Diagram

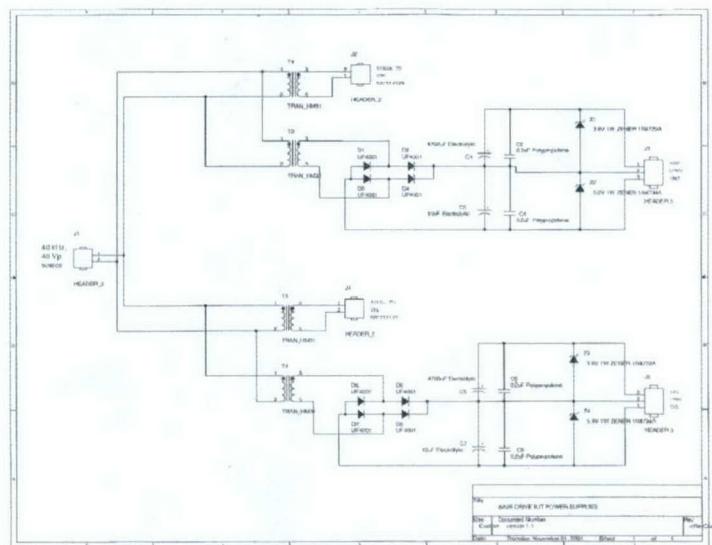


(b) Hardware implementation

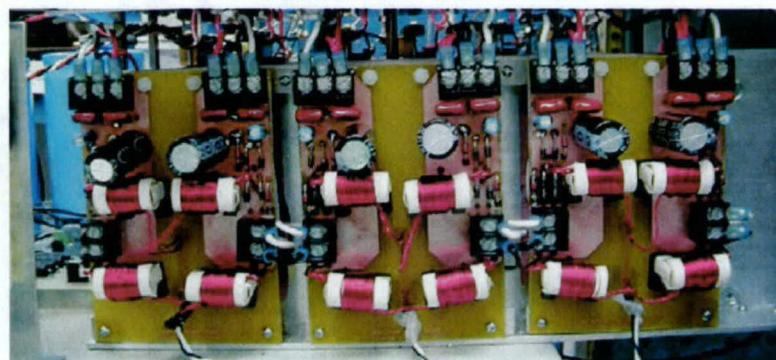
Fig. 38. Square Wave Power Supply

4.2.6.2 Gate Power Supply

The Gate Power Supply generates 1.6 V dc and -5 V dc levels used to turn the BJT on and off. To obtain these low voltage levels from the 40 V_p, 40 kHz source, ferrite core transformers are used. These transformers are quite small because of the relatively high frequency. The negative voltage needs to be applied to the base of BJT to provide negative base current at switch off to remove stored charge in the transistor for the purpose of fast switching. This negative base current must be the appropriate level to achieve minimal storage time and to prevent tailing of the collector current. It is important to maintain a negative base voltage during the switch-off interval to avoid unwanted switch-on which can be caused by capacitive coupling at high dv/dt. The schematic diagram and hardware implementation are illustrated in Fig. 39.



(a) Schematic Diagram

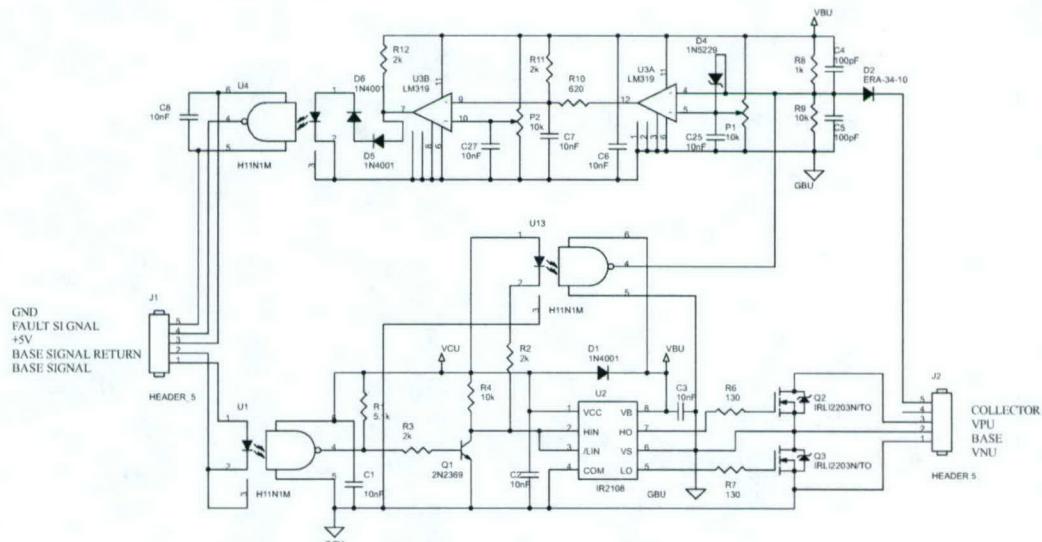


(b) Hardware implementation

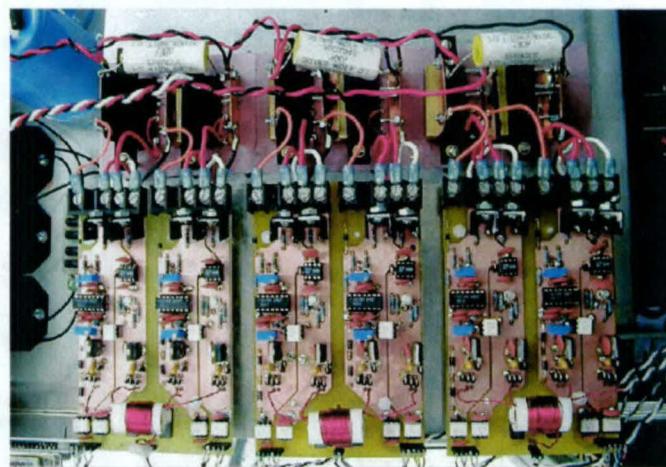
Fig. 39. Gate Power Supply

4.2.6.3 Switching Control Unit

The switching of the BJTs is controlled by this unit depending on the switching command signal which is generated by H-D modulator. To this end, the base of the BJTs is connected in a MOSFET based totem-pole configuration. To switch the two MOSFET used in totem-pole configuration, a high voltage, high speed power MOSFET driver IC is used. In particular, a IR2108 half-bridge IC is employed. Overcurrent protection is provided in the event of short circuit. Figures 40(a) and 40(b) illustrate the schematic diagram and hardware implementation.



(a) Schematic Diagram



(b) Hardware implementation

Fig. 40. Switching Control Unit

4.3 Steady State performance of the Test Bed

The performance of the test bed operated using silicon BJTs and silicon diodes is provided and depicted in Fig. 41, wherein the torque command is 10 Nm and speed is 141.3 rad/s. The resultant waveforms of the switching command signal to *a*-phase upper BJT, *a*-phase inverter current, and line-to-line inverter voltages are depicted.

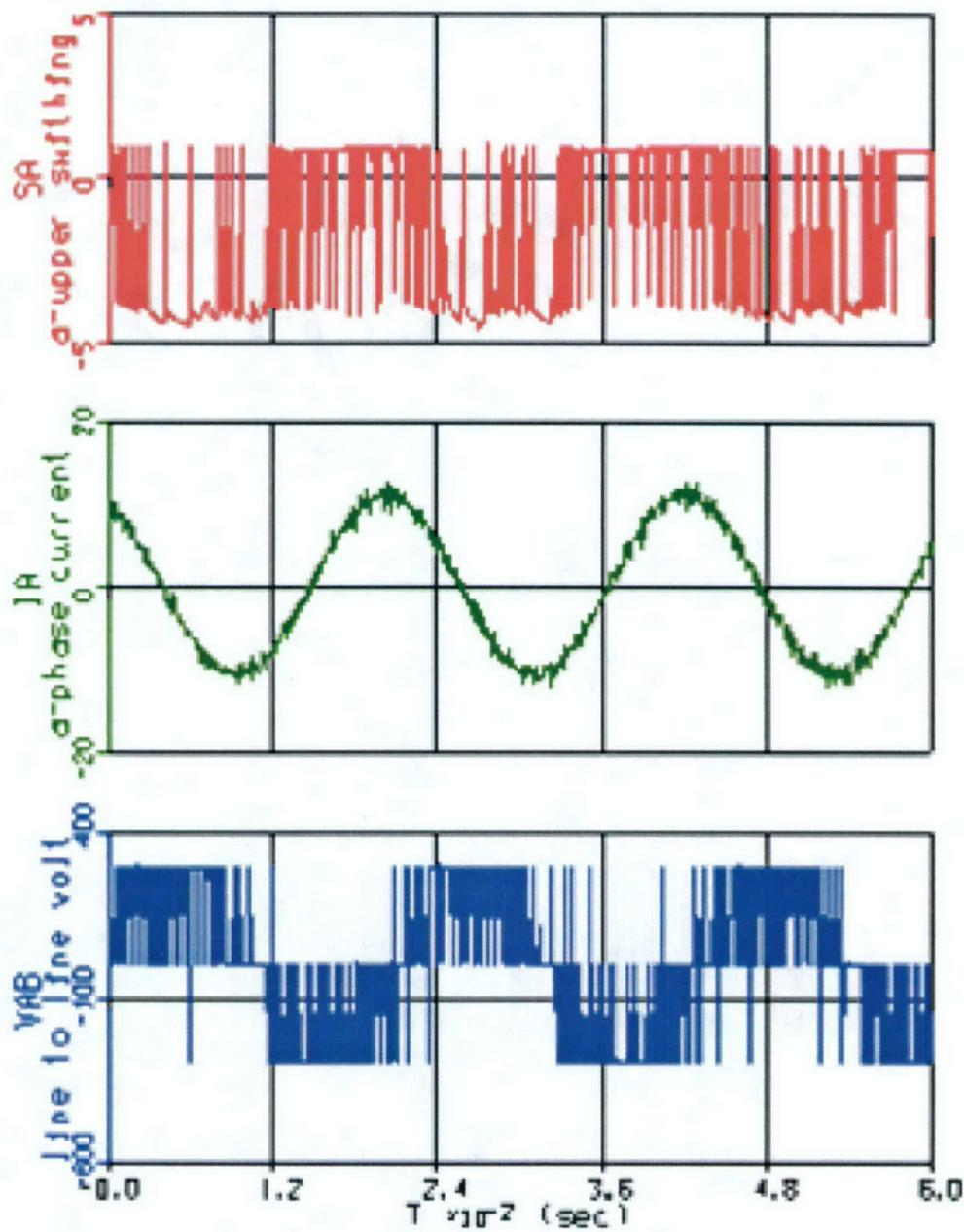


Fig. 41. The steady state performance of the test bed using silicon BJTs and diodes.

5. Project Summary

The goals of this project were: (1) to develop a design and processing sequence for high-power 4H-SiC bipolar junction transistors (BJTs) with blocking voltages above 1,000 V and on-state currents above 25 A; (2) to fabricate and package sufficient quantities of these devices to implement a demonstration motor control system; (3) to design and develop a prototype 40 kW motor control system for demonstrating the SiC BJTs; and (4) to operate the SiC BJTs in the prototype system as a real-world test of the feasibility of this technology for practical power conversion systems.

The project has been successful in each of its major components: (1) design and fabrication of SiC BJTs and PiN diodes capable of operation in the demonstration motor control system, and (2) design, construction, and demonstration of a motor control system capable of utilizing SiC BJTs and PiN diodes. The major failure of this program has been our inability to *package* the SiC components so that they could be operated in the system breadboard. The packaging activity was *not funded* as part of this project, and it was hoped that third party vendors could be persuaded to package a limited number of parts as a courtesy to the Navy. Unfortunately, the lack of a dedicated packaging effort within this program created difficulties that delayed the system demonstration.

At the time of this writing, the funded portion of the project has ended, but we are continuing our attempts to package some of the hundreds of SiC BJTs and diodes that have been produced. Cree, Inc. has agreed to package a limited number of these parts at no charge, and at the time of this writing, 17 BJTs and 10 diodes from the completed quarter-wafer of Wafer #4 are at Cree awaiting packaging. If packaging is successful, these devices will be inserted into the motor control breadboard and performance statistics recorded. Additional BJTs and diodes from Wafers #5 and #6 may also be packaged, if time permits. If meaningful performance data can be generated using the SiC parts, a supplemental report will be submitted to ONR, and results will be published.